A Comparative Analysis of Parallel Delta–Sigma ADC Architectures

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Abstract—Parallelism can be used to increase the conversion bandwidth of delta-sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs). Time-interleaved, parallel $\Delta\Sigma$, and frequency-band-decomposition ADCs are three parallel architectures that are shown to be explained using the same underlying theory. This common structure is then used to explore the design tradeoffs among these architectures. It is shown that the frequency-band-decomposition ADC is insensitive to channel mismatches but it is the most complex to design. The Hadamard modulated parallel $\Delta\Sigma$ ADC provides the best performance (without considering nonidealities) but requires large digital filters. Finally, a randomization technique is described that can be used with parallel $\Delta\Sigma$ architectures to spread out the tonal energy due to channel mismatches over the frequency spectrum.

Index Terms—Analog-to-digital converter (ADC), delta–sigma ($\Delta\Sigma$) converter, Nyquist rate ADC, parallel $\Delta\Sigma$, time-interleaved ADC.

I. INTRODUCTION

As communication devices infiltrate our home and work environments, there is continually a need to increase their performance while reducing the cost, size, and power. Whether the device is tailored to provide higher speed internet access to the home or wireless communication through a cellular phone, often the most challenging part of the overall design is the analog-to-digital converter (ADC). While it is possible to achieve very high speed analog-to-digital (A/D) conversion for low resolution [1], the bandwidth decreases dramatically for high resolutions [2].

Many new approaches to achieving both high speed and high resolution have been proposed. One approach is to extend the resolution of a Nyquist-rate ADC such as a pipelined converter by calibrating the converter [3]. The bandwidth can then be further extended by time-interleaving two pipeline converters [4]. Another approach is to use a very high resolution converter such as a delta–sigma ($\Delta\Sigma$) ADC and extend the bandwidth by reducing the oversampling ratio. To maintain high resolution with reduced oversampling, the converter order is increased, and/or multibit quantizers are used and/or parallelism is employed [5]. This paper focuses on various architectures that can be used to combine $\Delta\Sigma$ ADCs in parallel and thus reduce the oversampling ratio to extend the bandwidth of the oversampled converter while exploiting the high linearity of this architecture.

The most simplistic parallel $\Delta\Sigma$ ADC can be constructed by placing $\Delta\Sigma$ ADCs in parallel and applying the input signal to all of the channels simultaneously. The outputs from all of the channels are then digitally recombined to create the overall output. Using this direct approach, the resolution increases by only 0.5 bits for each doubling in the number of channels when the same bandwidth is considered. Thus, very little performance improvement is obtained for a significant increase in the area.

Two alternative approaches to combining $\Delta\Sigma$ ADCs in parallel are examined here. The first parallel $\Delta\Sigma$ ADC architecture analyzed in this paper is the frequency-band-decomposition ADC [6]–[8]. The general block diagram as in Fig. 1 can be used to describe this architecture. However in this architecture, no modulation or demodulation are not explicitly performed. The modulation is effectively performed internal to the $\Delta\Sigma$ modulator. In this architecture, each channel consists of a bandpass $\Delta\Sigma$ modulator with a quantization null at a different frequency. Thus, each channel passes one $\Delta$ of the signal frequency band when there are $M$ channels.

The second will be referred to as the modulation-based parallel $\Delta\Sigma$ ADC [9], [11]–[15]. In this architecture, the input signal and output signal are modulated and demodulated, respectively, as shown in Fig. 1. By modulating the signal at the input of each channel, the signal and quantization noise are effectively decoupled. As a result, the filter on each channel can be designed to filter the quantization noise while passing the signal to the output. Before obtaining the final output, the signal on each channel is demodulated and recombined. As will be shown in this paper, the performance that is obtained from this architecture depends on the modulation sequence applied to the signal. Other parallel $\Delta\Sigma$ ADC architectures also exist, but are beyond the scope of this paper [17]–[19].

In this paper, each of these parallel $\Delta\Sigma$ ADC architectures will be analyzed and it is shown that they can be described by the same underlying theory. The performance of the frequency-band-decomposition converter is analyzed in Section II and the filter criteria are derived. In Section III, the general theory for the modulation-based parallel $\Delta\Sigma$ ADC is derived. From this theory, the performance is obtained and the sensitivity to channel mismatches are described. To limit the tones generated by channel mismatches, a randomization technique is introduced in Section IV. Section V compares each of these architectures in terms of the theoretical performance and the tradeoffs in practical implementation. Finally, Section VI concludes the paper.
the quantization noise power of each channel and the signal-to-noise ratio (SNR) is

\[ \text{SNR} = 10 \cdot \log_{10} \left( \frac{P_S}{\sum P_{N_i}} \right) \] (1)

where \( P_S \) is the power of the signal and \( P_{N_i} \) is the quantization noise power of the \( i \)th channel.

In a conventional \( L \)th-order \( \Delta \Sigma \) ADC, doubling the oversampling ratio increases the resolution by \( L + 1/2 \) bits for low-pass or high-pass \( \Delta \Sigma \) modulators and \( L/2 + 1/2 \) bits for bandpass \( \Delta \Sigma \) modulators. In the design of the frequency-band-decomposition ADC, the first and the last \( \Delta \Sigma \) modulators will be low pass and high pass, respectively. All other channels will be bandpass. The zeros of the low-pass quantization noise transfer function are determined as in [20].

Assuming that the quantizer of the \( \Delta \Sigma \) modulator produces quantization noise which is white and uniformly distributed between \( \{-2\Delta, +2\Delta\} \), then, the mean square quantization noise of the \( i \)th channel is [21]

\[ \sigma_i^2 = \frac{2}{2\pi} \int_{-\omega_B}^{\omega_B} k^2 \omega - \omega_B)^{2L+1/2} \frac{L}{12} d\omega = \frac{\Delta^2}{12\pi^2} \left( \frac{\omega_{B}}{L+1} \right)^{L+1} (2) \]

for the bandpass \( \Delta \Sigma \). The low-pass (first channel) and high-pass (last channel) \( \Delta \Sigma \) modulator mean square quantization noise is

\[ \sigma_i^2 = \frac{1}{2\pi} \int_{-\omega_B}^{\omega_B} k^2 \omega^{2L+1/2} \frac{L}{12} d\omega = \frac{\Delta^2}{12\pi^2} \left( \frac{\omega_{B}}{L+1} \right)^{L+1} (3) \]

where \( \omega_B \) represents the frequency corresponding to the zeros of the quantization noise transfer function (i.e., \( e^{j\omega_B} \)) and the factor \( k \) accounts for the modulator poles [20].

In the above equations, the order of the bandpass \( \Delta \Sigma \) modulator is assumed to be \( L \) and the order of both the high-pass and the low-pass \( \Delta \Sigma \) modulators is assumed to be \( L/2 \). Note that if we assume that the high-pass \( \Delta \Sigma \) modulator is part of the low-pass \( \Delta \Sigma \) modulator, then (2) can be used as an estimate of the quantization noise for the bandpass or the combination of low-pass and high-pass \( \Delta \Sigma \) modulators. Making this assumption, the number of channels is effectively \( M-1 \) instead of \( M \).
Doubling the number of channels in this parallel $\Delta \Sigma$ ADC reduces the conversion bandwidth of each channel by half. For optimum performance, it is necessary to keep $k$ the same for all modulators so that the quantization noise for all frequency bands is the same. Thus, the total noise at the output of the ADC is

$$
e^2 = \sum_{i=0}^{M-2} e_i^2 = (M-1) \frac{N^2}{12\pi} k^2 \frac{\omega_B^{L+1}}{(L+1)}$$

where $M$ is the number of channels. Since the conversion bandwidth of each channel is

$$\omega_B = \frac{\pi}{2(M-1)}$$

the quantization noise power of the ADC as a function of the number of channels is

$$e^2 = \frac{N^2}{12} \frac{k^2 \pi^L}{(L+1)(M-1)^2}$$

For a given order of modulator $L$, doubling the number of channels attenuates the quantization noise by $(2M - 1)^L \approx 2L M^L$ which increases the resolution by $L$ bits.

Up to this point, the filter for this architecture has only been described as passing the null frequencies of the quantization noise filter. Next, it is shown that the optimal digital filter has the center tap set to $1/(M-1)$ and every $M$ taps are set to zero.

Let $H(z)$ be the filter frequency response for the low-pass $\Delta \Sigma$ of order $L/2$. Without loss of generality, we can assume that $H(z)$ has a reducible rational form of

$$H_{op}(z) = \sum_{n=-M}^{M} h_{op}[n] z^{-n}.$$  \hspace{1cm} (7)

For now we assume that filter $h_{op}[n]$ is normalized such that the center tap of the filter, which is $h_{op}[0]$ is $1/(M-1)$. The justification for this assumption is given at the end of this section. Since the auto-correlation of the quantization noise is an even function, the coefficients of $h_{op}[n]$ are symmetric. Therefore, the filter

$$H_k(z) = \sum_{n=-M}^{M} a_k \cdot h_{op}[n] \cos \left( k \cdot n \frac{\pi}{M-1} \right) z^{-n}$$

is an optimum filter for the $k$th channel of the frequency-band-decomposition architecture, where

$$a_k = \begin{cases} \frac{1}{2}, & \text{for } k \in \{0, M-1\} \\ 1, & \text{otherwise.} \end{cases}$$

The signal is filtered on each channel by the corresponding filter and if we let $h[n]$ represent the overall filter observed by the signal, then $h[n]$ can be written as

$$h[n] = \sum_{k=0}^{M-1} h_{op}[n] a_k \cos \left( k \cdot n \frac{\pi}{M-1} \right) = h_{op}[n] \sum_{k=0}^{M-1} a_k \cos \left( k \cdot n \frac{\pi}{M-1} \right).$$

The second summation is a scaled version of the comb sequence which is

$$\sum_{k=0}^{M-1} a_k \cos \left( k \cdot n \frac{\pi}{M-1} \right) = (M-1) \cdot c_{2(M-1)}[n] = \begin{cases} M-1, & n = \text{multiple of } 2(M-1) \\ 0, & \text{otherwise.} \end{cases}$$

(11)

To ensure that the signal sees an all-pass filter, the center tap of the $h_{op}[n]$ filter must be set to $1/(M-1)$ and every $M$th tap of the filter must be set to zero [11], [12]. As a result, the filter observed by the finite-impulse response (FIR) is

$$h[n] = \begin{cases} 1, & n = 0 \\ 0, & \text{otherwise.} \end{cases}$$

(12)

The justification for normalizing the center tap of the $h_{op}[n]$ filter to $1/(M-1)$ is that (2) and (3) are based on the assumption that the digital filter after the $\Delta \Sigma$ modulators are ideal bandpass filters.

The primary challenge in the frequency-band-decomposition ADC implementation is that each channel is unique and, as a result, the $\Delta \Sigma$ modulators and digital filters are different on each channel. This makes the design more complex, but as shown later in the paper, this architecture is less sensitive to channel matching than other parallel $\Delta \Sigma$ ADCs.

III. MODULATION-BASED PARALLEL $\Delta \Sigma$ ADCS

The frequency-band-decomposition parallel $\Delta \Sigma$ ADC converts a band of frequencies on each channel to achieve overall wideband conversion. The modulation-based architectures described in this section are a complex set of frequencies on each channel to achieve wideband conversion. Each of the modulation-based architectures are described by the general block diagram in Fig. 1. The name “modulation based” is used because the input and output are modulated by an external signal. It is referred to as the modulation sequence since the input is sampled prior to the modulation and the external signal is applied at discrete time steps. The signal at each time step is represented by a sequence of data. For the frequency-band-decomposition architecture, the modulation sequence is all ones and the actual modulation frequency is internal to the $\Delta \Sigma$ modulators. The general criteria for the modulation matrix in the modulation-based parallel $\Delta \Sigma$ ADC (where each channel corresponds to a row in the matrix and each column corresponds to a time instance) is that it is a unitary matrix. We will first show that a unitary matrix will allow the parallel $\Delta \Sigma$ ADC to convert wideband signals.

Let the sequence $u_t[n]$ be elements of a unitary matrix, where $\langle \rangle$ represents the modulo operation. Based on the linear model of the $\Delta \Sigma$ modulator, the signal path through the modulator is simplified as shown in Fig. 3(a). The input signal is first modulated by the input sequence $u_{t,n}^m$ and then enters the filter $h[n]$. The output of the filter is demodulated by a delayed version of $u_{t,n}^* m$ to account for the delay through the
For the ADC to be a Nyquist-rate ADC, the filter must satisfy
\[
h[n] = \begin{cases} 
1, & n = 0 \\
0, & n \text{ divisible by } M \\
\text{anything, otherwise.} & 
\end{cases} 
\] (16)

This defines the filter criteria with a unitary matrix for modulation. Once the criteria for the filter is established, the performance can be characterized by the expected power of the quantization noise. Note that the filter allows the signal to pass through without attenuation and, as a result, the power in the quantization noise will determine the overall resolution.

The overall quantization noise of the converter is determined by first representing the linearized quantization noise path for each channel as shown in Fig. 3(b). The input \( W[n] \) is the quantization noise on each channel. The symbol \( V(z) \) is the combination of the filter \( H(z) \), and the linearized quantization noise filter, \( N(z) \).

Assuming that the quantization noise among the \( \Delta\Sigma \) modulators are uncorrelated, the expected power of the quantization noise is
\[
e^2 = \left( \frac{1}{M} \sum_{i=0}^{M-1} \sum_{j=0}^{M-1} |u_{i,j}|^2 \right) \frac{\Delta^2}{12} \frac{1}{2\pi} \int_{-\pi}^{\pi} |V(e^{j\omega})|^2 d\omega. 
\] (17)

Thus, the mean-square power of the quantization noise is
\[
e^2 = \frac{\Delta^2}{12} \frac{\pi^2L}{2(2L+1)} \frac{1}{M^{2L+1}}. 
\] (18)

As (18) indicates, the total quantization noise power is independent of the unitary matrix used as the modulation basis. For every doubling in the number of channels, the bandwidth of the ideal low-pass filter reduces by a factor of two. A reduction in the bandwidth of the digital filter by a factor of two will attenuate the total quantization noise power by \( L \)-bits where \( L \) is the order of the \( \Delta\Sigma \) modulator. In the subsections that follow, three modulation-based architectures are described. The architectures are based on three different unitary matrices including the discrete Fourier Transform (DFT) matrix, the identity matrix and the Hadamard matrix.

A. DFT Modulation-Based ADC

The DFT matrix is one unitary matrix that can be used in the modulation-based parallel \( \Delta\Sigma \) ADC. This unitary matrix is shown here for an M-channel converter as shown in the equation at the bottom of the next page.

Each row in the modulation sequence is applied to one channel of the converter. The columns represent a particular time instance. The sequence is repeated by going back to the first column once the last column has been reached. Although it is impractical to realize a matrix such as this, the complex exponential of the DFT matrix helps to see the connection between the frequency-band-decomposition and the modulation-based architecture. The quantization noise power as shown in (17) applies to this unitary matrix. However, the overall performance is scaled by the \( 1/\sqrt{M} \) multiplier in front of the unitary matrix.

Since the signal entering each \( \Delta\Sigma \) modulator is modulated by \( (1/\sqrt{M})e^{j\omega n} \), the amplitude of the signal is attenuated by \( 1/\sqrt{M} \). This will result in an increase of \( \sqrt{M} \) in the \( \Delta\Sigma \) modulator dynamic range. Thus, the signal power at the output of the

\[ y[n] = \sum_{k=-L}^{L} h[k] \cdot x[n-k] \cdot C_M(k). \] (15)
modulation-based ADC has $M$-times more power than the frequency-band decomposition. However, this increase in the dynamic range is compensated by the center tap of the filter as shown in the appendix. We refer to this improvement in the dynamic range of the $\Delta\Sigma$ modulator as the coding gain which is 3 dB or 0.5 bit per doubling the number of channels. The major limitation of the DFT modulation-based architecture is that implementation of complex modulators are impractical.

**B. Time-Interleaved ADC**

The simplest unitary matrix is the identity matrix as shown below.

$$\begin{bmatrix}
1 & 0 & \cdots & 0 & 0 & 0 \\
0 & 1 & \cdots & 0 & 0 & 0 \\
\vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\
0 & 0 & \cdots & 1 & 0 & 0 \\
0 & 0 & \cdots & 0 & 1 & 0 \\
0 & 0 & \cdots & 0 & 0 & 1 \\
\end{bmatrix}$$

Fig. 4 shows a block diagram of the time-interleaved ADC [15]. Although the input to each channel is sampled at $1/M$ the clock rate, each modulator still operates at the full rate. Thus, the $\Delta\Sigma$ modulator requirements in terms of speed are not relaxed. During the time when the input is not being sampled, the input to the $\Delta\Sigma$ modulator is grounded. In this architecture, the signal travels down the shift register of the FIR filter. Once the sampled signal reaches the center tap of the FIR filter, the output of the FIR filter is sampled. Given that the FIR filters are the same on each channel and the signal is sampled from each channel when it reaches the center tap of the FIR filter, the overall transfer function of the architecture sees the center tap of the FIR filter and every four taps of the FIR filter. Thus, by setting every four taps of the FIR filter except the center tap to zero, the output signal is a delayed version of the input signal and the converter becomes a Nyquist-rate ADC.

**C. Hadamard-Modulated $\Delta\Sigma$ ADC**

Another version of the unitary matrix is the Hadamard matrix. An example of a $2 \times 2$ Hadamard matrix is

$$H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}.$$ 

Higher order Hadamard matrices can be generated using the recursive algorithm shown below

$$H_{n+1} = \frac{1}{\sqrt{2}} \begin{bmatrix} H_n & H_n \\ H_n & -H_n \end{bmatrix}. \quad (19)$$

An advantage of the Hadamard matrix is that the coefficients are made up of plus and minus ones. One can easily implement the Hadamard modulation by passing or crossing the differential signal as it was presented in [13]. The advantage of the Hadamard matrix is that the signal entering each channel is attenuated by $1/\sqrt{M}$. Thus, the dynamic range of the signal is extended by $\sqrt{M}$. Hence, the coding gain is 3 dB. One disadvantage of the Hadamard-modulated parallel $\Delta\Sigma$ is that the number of channels must be a multiple of two and the filters consume a significant amount of area.
IV. RANDOMIZATION IN THE PARALLEL ΔΣ ADC

Two types of randomization techniques are presented here that improve the spurious-free dynamic range of the Hadamard-modulated and the time-interleaved converters. In the Hadamard-modulated ADC, limit cycle oscillations may occur since the modulation sequence for the first channel is all ones. The input signal can be modulated by a pseudorandom sequence of \{+1, -1\} before entering the converter so that the input spectrum to the quantizer is whitened. To reconstruct the input signal at the output of the converter, the output of the converter is modulated by a delayed version of the same pseudorandom sequence that was used to modulate the input signal. This improves the overall performance, however, the drawback of the randomization technique is that the randomization works best with low to moderate resolution applications since the increase in the noise floor will significantly degrade a high resolution converter.

The underlying concept behind the parallel ΔΣ ADC is that the transfer function of the ΔΣ modulator is an integer number of unit delays. As a result, the input modulation term does not appear in the next data sample. Any deviation from this assumption results in the converter having a signal transfer function which is not an all-pass filter. Thus, the impulse response of the ΔΣ modulator exponentially decays. This exponential decaying behavior will appear as an added white noise at the output of the randomized Hadamard-modulated converter and it degrades the SNR. An advantage of the randomized converter is that the offset and distortion due to channel mismatch is also whitened by the output pseudorandom modulation technique. Thus, the randomized Hadamard-modulated parallel ΔΣ ADC compromises the SNR to achieve spurious-free dynamic range.

The mismatch in gain among channels of the time-interleaved ADC will result in signal images appearing at intervals of \(fs/M\). Although the pseudorandom modulation of the input and the output by a \(\pm 1\) sequence has proven to be effective in whitening the images generated by gain mismatches in the parallel ΔΣ, the same technique does not whiten the tones in the time-interleaved ADC.

To whiten the spectrum of images produced by channel gain mismatches, an extra channel must be used to randomize the selection of channels. We use a four-channel example to demonstrate the random channel selection algorithm shown in Fig. 5. Assuming eight tap FIR filters are used after the ΔΣ modulators, an extra channel can be used to eliminate periodic selection of the channels. In Fig. 5, a first-in–first-out (FIFO)
buffer is used to hold the unused channel. In order to obtain Nyquist-rate conversion, the signal should not be sampled more often than every four clock cycles onto each channel. The task of the FIFO is to guarantee that the selected channel will not be selected again until four clock cycles later. A temporary storage unit is used to keep the pointer selecting the extra channel. The switches $S_1$ and $S_2$ are used to switch the output of the FIFO into the temporary register and the output of the temporary register back into the input of the FIFO register or connect the output of the FIFO back into itself. As shown in Fig. 5(a), the output of the channel selector points to channel four. In the next clock cycle, the pointer to channel four is placed on top of the FIFO register and now the output of the channel selector points to the third channel. In this example, it is assumed that the pseudorandom bit generator indicated a change from $S_1$ to $S_2$. This causes the pointer to the third-channel to be stored onto the temporary regi-
V. COMPARISON OF THE PARALLEL $\Delta \Sigma$ ADCS

With the performance characterization from the Section IV, we can contrast and compare the different parallel $\Delta \Sigma$ A/D architectures. Table I summarizes the characteristics of each of the architectures. We begin by considering the frequency-band-decomposition converter. The suppression of the quantization noise for this architecture is a factor of two lower than the modulation-based architectures for the same order and number of channels. This is to be expected since for a single channel the same is true. However, the increase in resolution of $L$ bits for doubling the number of channels is the same as the modulation-based architectures.

A key advantage of the frequency-band-decomposition architecture is its insensitivity to channel mismatches. Since the signal is not modulated in this architecture, gain mismatches from channel-to-channel result only in frequency-dependent gain errors or ripple in the magnitude response. As a result, they do not introduce nonlinearities. The frequency-dependent gain errors result because the signal is filtered on each channel. The ripple in the magnitude is directly related to the channel gain mismatches, i.e., 1% gain mismatches result in a ripple of 1%. The offset on each channel is another source of channel mismatch. The frequency-band-decomposition architecture is insensitive to this offset since on all but the first channel (which is baseband) the offset is filtered out by the digital filter. The primary disadvantage of this architecture is the design complexity. Both the modulator and filter on every channel are unique. This requires a significant design effort especially for the analog modulator design. The digital filter, while different, can be easily synthesized.

The input-referred noise in the parallel $\Delta \Sigma$ ADC also presents interesting challenges. Each channel in the frequency-band-decomposition and Hadamard-modulation architectures must satisfy the overall system noise requirements. Although there are $M$ channels, the noise on each channel is effectively band-limited by a factor of $M$. Thus, as shown in Table I, the input-referred $KT/C$ noise on each channel must satisfy the overall system requirements.

Two very important considerations in every ADC are the sensitivity to sampling jitter and sampling input mismatches. In all of the parallel architectures, the jitter does not affect the linearity. However, if the jitter becomes too large, it will degrade the SNR. Mismatches in the sampling instances cause a frequency-dependent phase error. This will show up as ripple in the output with a step input applied. The time-interleaved and Hadamard-modulated architectures without randomization will produce signal-dependent tones due to both gain mismatches and offsets. The expressions for these are shown in Table I. The magnitude of the offset at the output is proportional to number of channels times the standard deviation of the offset. The magnitude of the channel mismatch tones relative to the signal is proportional to $1/\sqrt{M}$. It is important to note that there are $M - 2$ tones in the spectrum so the total noise power stays the same when the number of channels is increased. With randomization, the tones are whitened. This degrades the SNR slightly but improves the signal-to-noise-plus-distortion ratio (SNDR).

In both the time-interleaved and the Hadamard-modulation architectures, the signal sees only the center tap of the filter. This results in signal attenuation of 3 dB for every doubling in the number of channels. This is in contrast to the frequency-band-decomposition filter where the signal sees all the taps of the filter and, as a result, the signal amplitude is not degraded by the reduction in the filter bandwidth with the increase in the number of channels.

All of these architectures can use a combination of parallel channels with oversampling to increase the resolution without

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Offset</th>
<th>Channel Mismatch</th>
<th>Hardware Complexity</th>
<th>Coding</th>
<th>Filter Gain</th>
<th>Quantization Noise</th>
<th>$\frac{KT}{C}$ Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>FBD</td>
<td>$\sigma_o$</td>
<td>none</td>
<td>high</td>
<td>0</td>
<td>0 dB</td>
<td>$\frac{\sigma_o^2}{12} \frac{k^2}{L + 1} \frac{M^2}{(M - 1)^2} \frac{L}{2^{L+1}}$</td>
<td>$\frac{\sigma_o^2}{12} \frac{K^2}{L + 1} \frac{M^2}{(M - 1)^2} \frac{L}{2^{L+1}}$</td>
</tr>
<tr>
<td>TI</td>
<td>$\sigma_o \sqrt{1.41 \pi}$</td>
<td>$\sigma_o \frac{\sqrt{2 \pi}}{2}$</td>
<td>low</td>
<td>0 dB</td>
<td>-3 dB</td>
<td>$\frac{\sigma_o^2}{12} \frac{k^2}{L + 1} \frac{L}{2^{L+1}}$</td>
<td>$\frac{\sigma_o^2}{12} \frac{K^2}{L + 1} \frac{L}{2^{L+1}}$</td>
</tr>
<tr>
<td>Random TI</td>
<td>none</td>
<td>none</td>
<td>low</td>
<td>0 dB</td>
<td>-3 dB</td>
<td>$\frac{\sigma_o^2}{12} \frac{k^2}{L + 1} \frac{L}{2^{L+1}}$</td>
<td>$\frac{\sigma_o^2}{12} \frac{K^2}{L + 1} \frac{L}{2^{L+1}}$</td>
</tr>
<tr>
<td>Hadamard-Modulation $\Delta \Sigma$</td>
<td>$\sigma_o M \sqrt{1.41 \pi}$</td>
<td>$\sigma_o \frac{\sqrt{2 \pi}}{2}$</td>
<td>medium</td>
<td>3 dB</td>
<td>-3 dB</td>
<td>$\frac{\sigma_o^2}{12} \frac{k^2}{L + 1} \frac{L}{2^{L+1}}$</td>
<td>$\frac{\sigma_o^2}{12} \frac{K^2}{L + 1} \frac{L}{2^{L+1}}$</td>
</tr>
<tr>
<td>Random Hadamard-Modulated $\Delta \Sigma$</td>
<td>none</td>
<td>none</td>
<td>medium</td>
<td>3 dB</td>
<td>-3 dB</td>
<td>$\frac{\sigma_o^2}{12} \frac{k^2}{L + 1} \frac{L}{2^{L+1}}$</td>
<td>$\frac{\sigma_o^2}{12} \frac{K^2}{L + 1} \frac{L}{2^{L+1}}$</td>
</tr>
</tbody>
</table>
increasing the area. The characteristic of the architectures are the same for the oversampled versions. The only modification to Table I for oversampling is that the quantization noise and $KT/C$ noise for all architectures is reduced by the oversampling ratio.

**VI. CONCLUSION**

The underlying theory for several parallel $\Delta\Sigma$ ADCs has been described. It is shown that the frequency-band-decomposition converter is least sensitive to channel mismatches but requires large area for implementation and has lower gains for an increase in the number of channels. The modulation-based architectures are less sensitive to channel mismatch when randomization is applied.

**REFERENCES**


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