Jitter Analysis of High-Speed Sampling Systems

MITSURU SHINAGAWA, MEMBER, IEEE, YUKIO AKAZAWA, MEMBER, IEEE, AND TSUTOMU WAKIMOTO, MEMBER, IEEE

Abstract — This paper describes the jitter analysis of such practical sampling systems as A-to-D converters, sample-and-hold circuits, and samplers. A new model for estimating jitter is proposed. In this model, total jitter is composed of sampling circuit jitter, analog input signal jitter, and sampling clock jitter. Using this model, jitter is broken up into three components. To evaluate the model, a precise method for measuring jitter is devised. This method is based on sampling sine-wave signal-to-noise ratio calculations, and it enables separation of jitter and amplitude noise. Finally, the performance limit of converters is discussed as evaluated by the model.

I. INTRODUCTION

THE RECENT progress in LSI technology has resulted in major improvements in electronics. For A-to-D converters, in particular, not only a very high precision of over 90 dB [1] but also an ultrahigh speed of 2 GHz for 6 bits [2] have already been achieved. The accuracy and speed limitations of the converters are obviously important. The factors which limit the accuracy and speed of converters are jitter and harmonic distortion, or nonlinearity. The mechanism of harmonic distortion is well known, and there are many circuit designs to circumvent the problem. The mechanism of jitter, on the other hand, has not yet been clarified, and there are very few circuit designs dealing with the problem. Moreover, no precise jitter measurement method has been reported.

This is despite the fact that jitter is generally assumed to be the principal limiting factor. Progress toward high-precision and high-speed converters depends largely on reducing jitter. Against this background, our work on jitter modeling and estimation will be presented. First, a jitter estimation model [3], [4] for a practical sampling system will be proposed. In this model, signal generator jitter is given a definite expression. Based on this model, sampling circuit jitter is separated from signal generator jitter. To evaluate this model a precise jitter measurement method is presented. This method does not require precise delay adjustments between the analog input signal and the sampling clock, because it is based on sampled sine-wave signal-to-noise ratio (SNR) calculations. Finally, accuracy and speed limitations of the converters will be discussed based on the model. It will also be shown that the jitter suppression bandwidth is important for the design of high-precision, high-speed converters.

II. JITTER ESTIMATION MODEL

A. Test Sampling System: Sampler

Fig. 1 shows a circuit schematic of the specially designed sampler used for the sampling system in our experiments. The sampler consists of a GaAs Schottky barrier diode bridge with a bandwidth of 3 GHz. Cg is a hold capacitor.

There are two types of jitter in the sampling system. One is instability in the timing of the switch in the sampling gate. We have dubbed it sampling circuit jitter. Sampling circuit jitter is caused by the amplitude noise of both the sampler’s amplifiers and the sampling clock signal generator. The amplitude noise enters the sampling gate and its threshold fluctuates. It is well known that the amplitude noise of signal generators is very small, so we have neglected the signal generator’s amplitude noise effect.

The other is instability in the phase of the signal generators, which generate analog input and sampling clock signals. The phase instability is given by single-sideband (SSB) phase noise, which is caused by the oscillators, frequency dividers, multipliers, and amplifiers of the signal generators.

Sampler waveforms are shown in Fig. 2. The sampler is normally in the hold mode. When a very short pulse is applied to the clock input, a new sample is obtained. Jitter causes the sampling point to vary randomly, and this appears as voltage error. This voltage error also includes
amplitude noise, which is caused by the sampler’s amplifiers. These types of voltage errors must be separated for precise jitter estimation. The way in which separation is accomplished will be explained in more detail shortly.

A schematic of the sampling system is shown in Fig. 3. The system consists of three components: sampling circuit jitter, analog input signal jitter, and sampling clock jitter. We assumed that, since the bandwidth has limits, these limits would also reduce the signal generator jitter. In this model, this restriction is represented by two bandpass filters. These filters are inherent in the sampling circuit, and are thus constant and different from each other. The measured total jitter is given by the sum of these three components.

B. Signal Generator Jitter

Two signal generator jitter components can be expressed analytically. According to frequency stability theory [3], the square of the signal generator jitter, $\Delta t_{SG}$, can be expressed by

$$\Delta t_{SG}^2 = \frac{C}{f_c} \int_{f_t}^{f_c} L(f) \, df.$$  

Here, $L(f)$ is the SSB noise density at an offset frequency $f$, $f_c$ is the carrier frequency, and $C$ is a constant. This equation means that total phase instability is converted into timing jitter by the carrier frequency.

Bounds $f_c$ and $f_t$ give the bandwidth over which jitter is measured. Analog input signal jitter and sampling clock generator jitter are suppressed by this bandwidth. They depend on the particular sampling circuits, so we assume that they are constant. This bandwidth was represented in terms of a bandpass filter, as mentioned above, and so we have dubbed it the jitter suppression bandwidth.

If $L(f)$ is constant for different carrier frequencies, (1) implies that the jitter varies inversely with the carrier frequency. This condition is nearly satisfied in commercially available frequency synthesizers. The phase noise characteristic of the synthesizer used in our experiments is shown in Fig. 4 for an $f_c$ of 10 MHz. We obtained the same characteristics from 10 to 100 MHz by SSB phase noise precision measurements.

Thus, the signal generator jitter $\Delta t_{SG}$ can be expressed by

$$\Delta t_{SG}^2 = B (f_c) \frac{\Delta t_{SG0}^2}{f_c} = (f_c) \frac{\Delta t_{SG0}^2}{f_c}. \quad (2)$$

Here, $f_c$, $\Delta t_{SG0}$, and $\Delta t_{SG0}$ are normalized values. $B$ is the jitter suppression bandwidth function. In our experiments, it is difficult to estimate the jitter suppression bandwidth, so we used the last expression in the equation.

The measured voltage error distribution of a sampler acquisition operation is shown in Fig. 5. The plotted marks are measured values, and the solid line shows the Gaussian distribution. The measured distribution coincides with the theoretical Gaussian distribution, so jitter seems to conform to the law of Gaussian distribution. We assume that each jitter component can be approximated by a Gaussian distribution. Therefore, the total jitter can be estimated by
the sum of the squares of the three components:
\[ \Delta f^2 = \Delta t_s^2 + \left( \frac{f_{SIG0}}{f_{SIG}} \Delta t_{SIG0} \right)^2 + \left( \frac{f_{CLK0}}{f_{CLK}} \Delta t_{CLK0} \right)^2. \]

In this equation, we assumed that the sampling circuit jitter \( \Delta t_s \) is independent of the analog input signal and the sampling clock frequency because it is caused by instability in the timing of the switch in the sampling gate.

III. Precise Method for Measuring Jitter and Experimental Results

A. Sampled Sine-Wave Method

A block diagram of a conventional jitter measurement system is shown in Fig. 6. By taking several hundred thousand samples and calculating the standard deviation, the jitter can be estimated. It has been thought that signal generator jitter can be canceled, because the analog input signal and sampling clock, which are generated by the same signal generator, have the same jitter. However, jitter is a random quantity and the jitter suppression bandwidths are different from each other, so we assume that it is impossible to cancel signal generator jitter. Moreover, this method generates a large estimation error. This is because as the measurement is performed by sampling the analog input signal at its highest slew-rate point, precision delay adjustments between the analog input signal and the sampling clock are needed and precision slew-rate estimation is very difficult.

A new measurement method can eliminate the above problems. A block diagram of the new measurement method is shown in Fig. 7. The master clock drives two signal generators: one for the analog input and the other for the clock input of the sampler. This method is based on sampled sine-wave SNR calculations, so it does not require precision adjustments between the analog input signal and the sampling clock, and a precise slew-rate is easily yielded. We used (4) to determine the frequencies of the analog input signal and the sampling clock:
\[ f_{SIG} = mf_{CLK} + \Delta f. \]

Here \( \Delta f \) is the beat frequency, and \( m \) is an integer. A discrete Fourier transform (DFT) is very useful for calculating jitter. For example, we can use it to convert a finite-time sequence of sampled data into the frequency domain by means of a fast Fourier transform (FFT) algorithm. An FFT plot is shown in Fig. 8. The combined jitter and amplitude noise are observed as voltage error, which produces the noise floor. Therefore, the harmonics, which are not related to jitter, are excluded in the SNR calculations.

A flowchart of the new measurement method is shown in Fig. 9. First, the voltage error is separated into jitter and amplitude noise by method I, which uses discrete Fourier transforms. Next, the jitter is separated into its three components—sampling circuit jitter, analog input signal jitter, and sampling clock jitter—using method II. This is based on the jitter estimation model and (3).

B. Method I

The conversion factor for changing jitter to voltage error is the slew rate of the analog input signal. Specifically, for a sine-wave input, the slew rate is simply a cosine function. The new method is based on sampled sine-wave SNR
calculations, so we used its rms slope as the conversion factor. The instantaneous voltage of the sine wave, \( V(t) \), is written as \( A \sin(2\pi ft) \), where \( A \) is the amplitude from 0 to peak. For a given rms jitter \( \Delta t \), the voltage error is

\[
\frac{dV}{dt}_{\text{rms}} \times \Delta t = \sqrt{\int_0^T \left( \frac{dV(t)}{dt} \right)^2 dt} = \sqrt{2\pi fA \Delta t}
\]

and SNR can be expressed by

\[
\text{SNR} = 10 \log_{10} \left( \frac{A}{\sqrt{2}} \right)^2 \left( \frac{1}{\Delta t} + \frac{1}{\sqrt{2} \pi fA \Delta t} + e_v^2 \right).
\]

Here, \( e_v \) is the amplitude noise. It is clear that when the jitter term is much greater than the amplitude noise, \( A \) is large and SNR is independent of \( A \):

\[
\text{SNR} = -20 \log(2\pi f\Delta t).
\]

On the other hand, when the amplitude noise is much greater than the jitter term, then \( A \) is small and SNR is proportional to the logarithm of \( A \):

\[
\text{SNR} = 20 \log \left( A / \sqrt{2} e_v \right).
\]

These characteristics enable us to separate jitter from amplitude noise.

Fig. 10 shows an example of measurement results. Here we can see how accurate the model is. The horizontal axis is the amplitude of the analog input signal, and the vertical axis is SNR. The marks are measured values, and the curves were calculated for a total jitter of 5 ps and an amplitude noise of 145 pV. The measured values agree very closely with our model.

C. Method II

The total jitter of a practical sampling system is given by (3). There are three unknown quantities: sampling circuit jitter (\( \Delta t_s \)), analog input signal jitter (\( \Delta t_{SG0} \)), and sampling clock jitter (\( \Delta t_{CLK0} \)). We can thus obtain the value of each component by treating the total jitter as three sets of different analog input signals and sampling clock frequencies. The results are listed in Table I. Substituting these measured total jitter values into (3), we obtain 2.97 ps for \( \Delta t_s \), 3.04 ps for \( \Delta t_{SG0} \), and 2.62 ps for \( \Delta t_{CLK0} \) for an \( f_{CLK0} \) of 40 MHz and an \( f_{CLK0} \) of 20 MHz.

To check the accuracy of the method, we measured the total jitter for an \( f_{SIG} \) of 60 MHz and an \( f_{CLK} \) of 15 MHz and then calculated it by substituting these values into (3). The calculated value of 5.01 ps agrees well with the measured value of 5.09 ps. This confirms the validity of the jitter estimation model and the measurement method.

IV. DISCUSSION

What does our new model have to say about the performance limit of converters? We assume that there are no harmonics and no amplitude noise. The converter operates up to the Nyquist frequency (\( f_{NSC} = f_{CLK}/2 \)). The total jitter is given by

\[
\Delta t^2 = \Delta t_s^2 + \Delta t_{SG0}^2 = \Delta t_s^2 + \left( \Delta t_{SG0} \left( f_{CLK0} / f_{CLK} \right) \right)^2.
\]

For an \( f_{SG0} \) of 5 MHz and an \( f_{CLK0} \) of 10 MHz, from the measured value a \( \Delta t_s \) of 2.97 ps and a \( \Delta t_{SG0} \) of 24.9 ps are obtained. When \( f_{CLK} \) is very high, \( \Delta t_s \) is much greater than \( \Delta t_{SG0} \), and SNR is given by

\[
\text{SNR} = -20 \log_{10} \left( \frac{\pi f_{CLK} \Delta t_s}{2} \right)
\]

where, as \( f_{CLK} \) increases, SNR decreases by 20 dB/dec. When \( f_{CLK} \) is very low, \( \Delta t_s \) is much smaller than \( \Delta t_{SG0} \), and SNR is given by

\[
\text{SNR} = -20 \log_{10} \left( \frac{\pi f_{CLK} \Delta t_{SG0}}{2} \right)
\]

where SNR is independent of \( f_{CLK} \).

Our predictions are summarized in Fig. 11. The horizontal axis is the sampling frequency, and the vertical axis is.
SNR. The solid line is the performance limit of the sampler we studied. This 62 dB is relatively small and is inconsistent with the reported SNR of a 90-dB audio band converter [1]. However, this discrepancy could be due to a difference in the jitter suppression bandwidth of the converters. We obtained the broken lines by independently varying signal generator jitter ΔfSG and sampling circuit jitter ΔfS. The lines show the acceptable values of each jitter component for a given accuracy and speed. It should be noted that ΔfS reduction has a practical effect on ΔfSG by a jitter suppression bandwidth change and thus should be taken into account in deriving these curves. It is probable that in the high sampling frequency region the jitter suppression bandwidth will become wider.

It is seen that, for converters in the high sampling frequency region, the sampling circuit jitter must be reduced, and in the low sampling frequency region, the signal generator jitter must be reduced. This indicates the importance of incorporating an appropriate jitter suppression bandwidth into the design. This figure also predicts a measurement limitation of the converter using frequency synthesizers that are commercially available.

V. CONCLUSION

We have proposed a new model for estimating jitter in a practical sampling system. This model includes sampling circuit jitter and signal generator jitter, and it provides a way of measuring jitter precisely by breaking it up into three components. To evaluate this model, we have devised a precision jitter measurement method based on sampled sine-wave SNR calculations. Based on this model, we have formulated guidelines for designing advanced converters.

ACKNOWLEDGMENT

The authors are greatly indebted to A. Ishida, T. Sudo, and A. Iwata for their useful suggestions and comments.

REFERENCES


Mitsuru Shinagawa (M'87) was born in Niigata, Japan, on June 1, 1960. He received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1983 and 1985, respectively.

In 1985 he joined the Electrical Communication Laboratories, Nippon Telegraph and Telephone Corporation (NTT), Tokyo, Japan. He is currently engaged in research on ultra-high-speed IC's at the NTT LSI Laboratories, Kanagawa, Japan.

Mr. Shinagawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Yukio Akazawa (M'87) was born in Yokohama, Japan, on July 26, 1940. He received the B.S. degree in electronic engineering from Yamagata University, Yonezawa, Japan, in 1967.

He is a Senior Research Engineer Supervisor at the NTT LSI Laboratories, Kanagawa, Japan. There he is presently engaged in the research and design of A-to-D and D-to-A conversion LSI's. Since joining the NTT system in 1973, he has been engaged in the research and design of high-speed logic LSI's, CMOS analog LSI's, and gigahertz-band IC amplifiers using GaAs and Si bipolar technology for telecommunication use.

Mr. Akazawa received the Outstanding Paper Award at the 1978 IEEE International Solid-State Circuits Conference, the NTT President's Award in 1980, and the IEEE JOURNAL OF SOLID-STATE CIRCUITS' Best Paper Award in 1987. He is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Tsutomu Wakimoto (M'88) was born in Ehime, Japan, on March 27, 1955. He received the B.S. and M.S. degrees in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 1978 and 1980, respectively.

In 1980 he joined the Nippon Telegraph and Telephone Public Corporation (NTT), Tokyo, Japan. He has been engaged in the research of gigahertz-band amplifier IC's using GaAs MESFET and Si bipolar technology for telecommunication use. He is currently involved in the research of high-speed Si bipolar analog-to-digital conversion LSI's and high-speed, high-resolution sample-and-hold circuit IC's.

Mr. Wakimoto received the IEEE JOURNAL OF SOLID-STATE CIRCUITS' Best Paper Award in 1987. He is a member of the Institute of Electronics and Communication Engineers of Japan.