Chapter 3

NYQUIST-RATE A/D CONVERTER ARCHITECTURES

This chapter deals with the architecture, features and limits of Nyquist-rate analog/digital converters. We shall start with the full-flash architecture capable to obtain the conversion in only one clock period. Following, we shall study the two-step solution which algorithm requires at least two clock periods to be accomplished. Next, we shall discuss folding and the interpolation methods. The interleave technique permits the designer to take advantage of the cooperative action of many converter working in parallel. We shall consider benefits and limit of this approach. Then we shall analyse the successive-approximation algorithm. The sequential algorithms are suitable pipeline architecture: they are popular methods for communication systems. Finally, we shall consider some special techniques.

3.1 INTRODUCTION

The sampling frequency of a Nyquist-rate data converters is normally near the Nyquist limit. This choice, as discussed in Chapter 1, leads to complex anti-aliasing specifications. The order of the antialiasing filter can be more than
three or four; however, using a reduced sampling rate can lead to less power consumption and ensure an optimal use of the bandwidth of analog circuits.

The maximum signal band that a converted can handle depends on the $f_T$ of the technology. To find the relationship between maximum input band and $f_T$, we start observing that the antialiasing filter requires a given margin, $\alpha$, from signal band to clock frequency. Moreover, the maximum usable clock depends on the speed of analog processing. If the algorithm needs op-amps they are the limiting factor. The unity gain bandwidth ($UGB$) of an op-amp must be $\beta$ times smaller than the technology $f_T$. Moreover, a proper settling of signals imposes a margin $\gamma$ between the op-amp $UGB$ and the clock frequency. Finally, the algorithm needs a given number of clock periods, $k$, to perform the conversion. Summing up, the maximum signal band is $f_T/(\alpha \beta \gamma k)$. Thus, for example, a technology which $f_T$ is 21 GHz enables designing op-amps with $UGB = 2.1$ GHz ($\beta = 10$). For medium resolution the settling imposes a margin $\gamma = 7$; the clock frequency becomes 300 MHz. The use of an algorithm requiring two clock periods per conversion lead to 150 MS/s. Nyquist is at 75 MHz. Assuming an antialiasing margin $\alpha = 2.5$ the input bandwidth becomes 30 MHz. The transition band of the antialiasing filter is from 30 MHz to 120 MHz corresponding to two octaves from the pass-band to the stop-band.

The ADC timing accounts for input sampling, implementation of conversion algorithm, and output code generation. As mentioned before these operations can need one or more clock cycles. When the converter uses only one clock cycle the architecture is full-flash. A two-step flash or folding needs two (or three) clock cycles. Many clock cycles are necessary for successive approximation techniques and for some algorithmic converters.

Conversion algorithms requiring many clock cycles normally are more accurate, require low power and consume less chip area than counterparts that utilize one or two clock periods. The throughput of slow converters is increased by using the interleaved or the pipeline architectures. Interleaved converters employ many converters that process in parallel successive samples of the input. Pipeline architectures exploit a cascade of elementary blocks capable to sequentially determine one or more bits per stage. The throughput of the interleaved or the pipeline solution is high but a given latency time features the results.

### 3.2 TIMING ACCURACY

The inaccuracy of the sampling time (sampling-time jitter) critically affects the dynamic performances of high-speed Nyquist-rate data converters. To preserve performances the jitter error of an for $n$-bit converter must be less than $1/2$ LSB, $V_{FS}/2^{n+1}$. The jitter error was studied in Chapter 1. Here we just recall
3.2. Timing Accuracy

That the sampling error is proportional to the derivative of the input signal

\[ \delta V_{in} = \delta T_{ji} \cdot \frac{dV_{in}}{dt} \]  

(3.1)

For 1 V peak sine wave at 20 MHz an error lower than 0.1 mV requires a time jitter below 1 psec. Thus, it is necessary to put great attention on clock generation and phase distribution when the resolution is, for example, more than 12-bit and the input frequency is few ten of MHz.

Sources of timing inaccuracy are the jitter and the finite rise/fall time of the clock, the propagation delay, and signal dependent delays. The main clock jitter is given by a the clock generator. Some applications use a sine wave as clock and square the signal inside the chip. This approach leads to high spectral purity but the finite slope at zero crossings and the transistors’ noise make uncertain the sampling times. In this case it is important to design the amplifiers used for squaring with low-noise.

The propagation of digital signals along metal interconnections causes dispersion and delay. Fig. 3.1 shows a simplified distributed RC model of the interconnections. The response to a step signal with finite rise-time

\[ e_i(t) = \frac{E}{T_R} t \quad \text{for} \quad 0 \leq t \leq T_R \]
\[ e_i(t) = E \quad \text{for} \quad t > T_R \]  

(3.2)

is given by [10]

\[ e_{out}(t) = V_r(t) - V_r(t - T_r) \]  

(3.3)

\[ V_r = \frac{E}{T_R} \left\{ \frac{t + \frac{\tau}{2}}{2} \left[ 1 - \text{erf} \left( \frac{\frac{\tau}{\sqrt{4t}}}{\sqrt{\frac{\tau}{2}}} \right) - \frac{\tau}{\sqrt{\frac{\tau}{2}}} e^{-\frac{\tau}{4t}} \right] \right\} \]  

(3.4)
where \( V_r \) is an intermediate function and \( \tau = R_u C_u L^2 \).

The delay is roughly calculated by

\[
T_D = \tau = R_u C_u L^2 \tag{3.5}
\]

where \( R_u \) and \( C_u \) are the resistance and capacitance per unity length.

Observe that if the width increases the resistance per unity length decreases but the capacitance per unity length increases by the same extent. Therefore, the delay does not change if the width of interconnections are enlarged. For a typical submicron technology the value of the product \( R_u C_u \) is in the order of some \( 10^{-17} \, \text{s/}\mu^2 \). Few hundreds of micron of interconnection can produce a delay in the order of 1 ps.

**Example 3.1**

Use equations (3.3) and (3.4) to estimate the clock waveform after 150\( \mu \) and 300\( \mu \) of metal interconnections. \( R_u = 0.02\,\Omega/\mu \) and \( C_u = 2.5 \times 10^{-16} \, \text{F/}\mu \). The rise time of the clock is 50 fsec. Determine the clock slope at half of the full-amplitude.

**Solution:** The file Ex3_1 provides the basis for the computer evaluation of the responses. Fig. Ex. 3.1 gives the waveforms. Equation (3.5) estimates the value of \( \tau \). It is 0.225 psec and 0.9 psec for

![Fig. Ex. 3.1 - Clock waveform after a 150\( \mu \) and 300\( \mu \) metal line.](image-url)
3.2 Timing Accuracy

150\(\mu\) and 300\(\mu\) metal interconnection respectively. The values are close to the ones of the figure at half of the full-amplitude. The slopes are 0.98 \(V_{FS}/\text{psec}\) 0.28 \(V_{FS}/\text{psec}\) respectively. Thus, a noise of 10 \(mV_{FS}\) in the crossing threshold would cause a jitter of 9.8 fs and 2.8 fs respectively.

3.2.1 Metastability error

Metastability error occur when the output of a comparator is undefined. Typically a gain amplifier and a latch (Fig. 3.2) make a sampled-data comparator. During one phase the input signal is pre-amplified and during the latch phase a regenerative circuit fixes the logic level. If the input differential voltage, \(V_{in,d}\), is not large enough the comparator output may be undefined at the end of the latch phase. An undefined state leads to an error in the output code and possibly causes code bubble error.

The differential latch of Fig. 3.2 is the positive loop of two transconductors. The regenerative time constant, \(\tau\), is

\[
\tau = \frac{C_p}{g_m}. \quad (3.6)
\]

The metastability error probability [4] can be approximated by

\[
P_E = \frac{V_0}{V_{in,d} A_0} e^{-t_r/\tau} \quad (3.7)
\]

where \(V_0\) is the output voltage swing required for valid logic levels and \(t_r\) is the time slot for the latch operation. Since \(t_r\) equals \(1/(2f_s)\) the metastability error increases exponentially with sampling frequency. Moreover, the error is

Fig. 3.2 - Typical comparator used in data converters.
inversely proportional to the differential input amplitude, $V_{in,d}$. The maximum $V_{in,d}$ is half the quantization step. Therefore, a given $P_E$ require using a latch period, $1/(2f_s)$, proportional to $\tau$ and the number of bits.

### 3.3 FULL-FLASH CONVERTERS

The basic function of an analog-to-digital converter is to identify the quantization interval that contains the input signal. A direct way to achieve the operation is to compare the input signal with all the transition points between consecutive bins. The result of all these comparisons marks the limit at which the input is larger than one of the thresholds; the information is then translated into a digital code. This “brute force” (but effective) approach leads to full-flash architectures. The name of the algorithm comes from the fact that all the comparators operate in parallel and procure the result in one clock period.

The input signal is sampled and held before the parallel action of comparators. An $n$-bit converter identifies $2^n$ bins. The transition points are $2^n - 1$. Therefore the architecture, as shown in Fig. 3.3, requires $2^n - 1$ reference voltages and $2^n - 1$ comparators. The comparators generate a logic 1 up to a given output. The outputs become a logic 0 when the reference voltage exceeds than input. The set of output signal composes a thermometric representation of the digital result. A ROM decoder translates the thermometric input into an $n$-bit digital output.

#### 3.3.1 Reference Voltages

The simplest way to generate the reference voltages is to use a resistive divider connected between the positive and negative reference voltages, $V_{ref^+}$, $V_{ref^-}$. All the resistors are nominally equal. Some implementations (like the one shown in Fig. 3.3) use $R/2$ as ending elements. In this case the the $i$-th reference voltage is given by

$$V_r(i) = V_{ref^-} \cdot \frac{i-\frac{1}{2}}{2^{n-1}} (V_{ref^+} - V_{ref^-}); \quad i=1, 2^n - 1; \quad (3.8)$$

the first quantization interval and the last one are half $\Delta$. The quantization step equals the dynamic range divided by $2^n - 1$. Thus, $\Delta = (V_{ref^+} - V_{ref^-})/(2^n - 1)$.

The resistances of the voltage divider are nominally equal. However, random and systematic errors affect integrated resistors. The resistances must be made by the same kind of material: this to ensure a good matching accuracy. For integrated technologies the matching is in the order of 0.1-0.2%. The random mismatch is not a limit up to 10-bit of accuracy.
A possible gradients in the specific resistance causes integral non-linearity. If, for example, the resistors are laid out as a single straight sequence the gradient on resistances makes the resistors on one side of the string larger than the value on the other side. The drop voltage on the resistors increases linearly, thus leading to second order distortion terms. When the layout is bented in two segments the gradient augments the resistor values in half of the string and brings the value of the resistor back to the initial value in the second half. The result is an s-type (third order) distortion response.

**Example 3.2**

The resistive divider of a full-flash ADC is made by $2^n$ 50 Ω resistors. The technology is a CMOS 0.5 μ. Polysilicon makes the resistors. The specific resistance is 25 Ω/μ. Assume that the polysilicon resistivity is affected by a 300 ppm/μ linear gradient. Estimate the INL for different layout styles.

**Solution:** The accuracy of the unity resistance depends on the size
of the strip. Fig. Ex 3.2 a) uses for the resistance 2 squares of poly 2.5 x 5 μ. The width is 5 times the minimum feature. The value is likely enough to ensure a good matching. Fig. Ex 3.2 b) shows the layout of a resistive divider made by a single straight sequence. The first and the last element are 25 Ω, we obtain that value with one square of polysilicon. Other resistances are two square. The resistance pitch is 7μ leading to a total length of 470 μ. Assume that the resistance at the beginning of the string equals the nominal value, at the end of the string it is 1.14 the nominal value. The file Ex3_2 permits to analyze the problem by computer simulations. The estimated the INL is around 1 LSB.

Fig. Ex 3.2 c) shows a more compact layout. It uses the same unity resistance but the resistance pitch is 3.5 μ.

Fig. Ex 3.2 d) folds the single straight sequence of Fig. Ex 3.2 c) in two parts. Neglecting gradient effect in the vertical direction, the resistor value at the beginning and end of the string are equal. Computer simulations show that the reduction of the resistance
3.3. Full-Flash Converters © F. Maloberti

pitch to 3.5 μ diminishes the INL to 0.5 LSB. The folding leads to an s-type INL which maximum is 0.125 LSB (Fig. Ex. 3.2 e).

A possible temperature gradient along the resistive divider causes error. The temperature coefficient in integrated resistors depends on the material used and can be as large as 10,000 ppm/°C. Thus, a linear temperature drift of 7° along the string gives rise to 1 LSB INL for a 7-bit ADC.

The reference voltages at various taps of the resistive divider bias the input of the comparators. The loads are not static. The comparators can operate in a continuous-time or in a sampled-data fashion. Both modes establish a coupling between taps of the resistive network and the input terminal. Because of the coupling a sudden variation of input modifies the reference voltages. Resistors must be able to bring back the references with less than 1/2 LSB error. The time allowed is less than half sampling period. So, the time constant associated to resistance and parasitic coupling must be much smaller than the recovery time, especially for medium-high resolution.

Example 3.3

Simulate the transient response of the resistive divider of a 7-bit full-flash converter. The divider is made by 128 equal 50 Ω resistors. The coupling between every resistive taps and input is 12.5 fF. Sampling frequency and input band are such that the maximum input variation is half reference voltage, \( V_{\text{ref}} = 1 \text{ V} \).
Solution: The equivalent network modeling the resistive divider is an RC ladder made by 128 cells (Fig. 3.3 a). We have too many cells for computer studies. The circuit can be simplified by grouping a number of cells (16) and using an approximate T equivalent. The Spice simulation of the simplified circuit leads to the transient responses shown in Fig. 3.3 b). The input signal switches from 0 to 0.5 V. The capacitive couplings push all the reference voltages up by 0.5 V. Then, the low impedance $V_{\text{ref}}$ and ground bring down the reference voltages to the nominal values. The middle point reference $V_r(64)$ reaches half LSB accuracy after 5.6 ns. Since $V_r(112)$ is closer to the low impedance point $V_{\text{ref}}$ it achieves half LSB accuracy range in a shorter time interval (4.4 ns).

Fig. Ex. 3.3 a) - Equivalent circuit of the resistive string and its simplification.

Fig. Ex. 3.3 b) - Transient response at the middle point and the resistance # 112.
3.3.2 Offset of Comparators

The input referred offset of comparators affects the accuracy of a full-flash converter. The offset of the generic \(i\)-th comparator is represented by an additive term, \(V_{os,i}\), superposed to the input. With offset the output logic state changes when the input exceeds \(V_r(i) - V_{os,i}\) instead of \(V_r(i)\). Consequently, the \(i\)-th quantization interval becomes

\[
\Delta_i = \Delta - V_{os,i} + V_{os,i-1}. \quad (3.9)
\]

In order to ensure no missing codes or non-monotonicity the offset must be less than \(1/2\)-LSB. For example, the LSB of an 8-bit data converter with \(V_{FS}=1V\) is 3.4 mV. The offset must be 1.7 mV or less.

The offset is normally caused by the first gain stage of the comparator. A proper design and layout avoids the systematic offset. The mismatch of the threshold voltage in input differential pair and the mismatch in the active loads are responsible of the unavoidable random offset. The standard deviation of the \(\Delta V_{Th}\) threshold mismatch in a pair of MOS transistors is given by

\[
\sigma_{\Delta V_{Th}} = \frac{A_{VT}}{\sqrt{WL}} \quad (3.10)
\]

where the constant \(A_{VT}\) depends on technology. For a 0.18 \(\mu\) CMOS process \(A_{VT}\approx 2mV/\mu\) (a 0.2 mV offset requires, for example, a \(W/L=500\mu/0.2\mu\)).

The mismatch of the active load causes an input referred offset equal to the global mismatch \(\Delta x_{AL}/x_{AL}\) multiplied by \(I_{DS}g_m\) (current and transconductance of the input pair). For an MOS in saturation \(I_{DS}g_m = (V_{GS}V_{Th})/2\). The standard deviation of the MOS offset sums up

\[
(\sigma_{V_{os}})_{MOS}^2 = \left(\frac{A_{VT}}{\sqrt{WL}}\right)^2 + \left(\frac{V_{GS}-V_{Th}}{2}\right)^2 \left\{\sigma\left(\frac{\Delta x_{AL}}{x_{AL}}\right)\right\}^2. \quad (3.11)
\]

The bipolar counterpart of (3.11) is the sum of two terms one describing the the \(V_{BE}\) mismatch and the second the active load mismatch

\[
(\sigma_{V_{os}})_{BJT}^2 = (\sigma_{V_{BE}})^2 + V_T^2 \left\{\sigma\left(\frac{\Delta x_{AL}}{x_{AL}}\right)\right\}^2. \quad (3.12)
\]
The mismatch between $V_{BE}$ of bipolar transistors is negligible: a mismatch in the emitter area determines a difference in emitter currents. The error on $V_{BE}$ is given by $\Delta V_{BE} = V_{BE} \log((I_E + \Delta I_E)/I_E)$. Moreover, the multiplying factor $V_T = 26 \text{ mV}$ is 2-5 times smaller than the CMOS counterpart $(V_{GS} - V_{Th})/2$. Therefore, the CMOS offset can be larger by a 5 or more than the bipolar offset.

**Example 3.4**

Estimate the standard deviation of the offset of a CMOS and its bipolar comparator. The MOS transistor of the input pair preamplifier are $W/L = 6 \mu m/0.18 \mu m$. The $g_m$ is 800 $\mu A/V$ and the bias current is 80 $\mu A$. The technology is 0.18 $\mu m$ CMOS with $A_{VT} = 2 mV$. The active load mismatch is $\sigma(x_{AL}/x_{AL}) = 0.4\%$. The bipolar preamplifier uses the same bias current. The load mismatch is the same as the CMOS load mismatch. The error on the emitter area is 0.2\%.

**Solution:** Remember that the overdrive voltage of MOS transistors is $(V_{GS} - V_{Th}) = 2I_D/g_m$. Equation (3.11) leads to

$$\sigma_{V_{os}, MOS} = \frac{2 \cdot 10^{-3}}{\sqrt{33.3}} + \left(\frac{0.08}{0.8}\right)^2 \cdot 1.6 \cdot 10^{-5} = 0.52 \text{ mV}$$

The two mismatch terms are close: 0.34 mV and 0.4 mV. The current in bipolar transistors changes exponentially with $V_{BE}$: $I_E = A_{ss} \exp(V_{BE}/V_T)$. (A emitter area.) Eq. (3.12) leads to

$$\sigma_{V_{os}, BJT} = 26 \cdot 10^{-3} \sqrt{\ln(1.002)^2 + 1.6 \cdot 10^{-5}} = 0.116 \text{ mV}$$

Observe that the area mismatch causes 0.05 mV offset while the load mismatch leads to 0.1 mV offset.

### 3.3.3 Offset Auto-zeroing

The auto-zero technique compensates for the offset of comparators. The method, accomplished in a sampled-data fashion, requires two phases of operation. One phase is used to measure the offset; the other phase enables the offset cancellation. Fig. 3.4 show a possible circuit implementation. During
phase $\Phi_{AZ}$ the amplifier is in unity gain configuration and makes it available the offset at the inverting input. The capacitor $C_{OS}$ is charged to the offset minus the input voltage $V_i$. During the complementary phase, $\Phi_{AZ}$, the amplifier is in open loop configuration and the capacitor $C_{OS}$ operates like a level shifter equal to $V_i - V_{OS}(\Phi_{AZ})$. The differential input is

$$V_{d,in} = V_+ - V_- = V_{OS}(\Phi_{AZ}) - V_2 + [V_1 - V_{OS}(\Phi_{AZ})]. \quad (3.13)$$

If the offset does not change during an entire period the circuit achieves offset cancellation. Opening the switch connected in feedback leads to charge injection into $C_{OS}$ (clock feed-through). With proper compensations techniques the offset can be reduced to fractions of mV. Also, the $1/f$ noise is attenuated.

Full-flash architectures use the offset cancellation scheme of Fig. 3.4. One terminal is connected to a tap of the resistive divider and the other terminal is connected to the input. Thus, terminals $V_2$ and $V_1$ take the role of the differential inputs of the comparators of Fig. 3.3. Observe that the parasitic capacitance at the left plate of $C_{OS}$ (node $A$, Fig. 3.4) establishes a coupling between the two inputs. The voltage across the parasitic is the input voltage during $\Phi_{AZ}$; when $\Phi_{AZ}$ goes on the voltage of node $A$ switches to the reference. Therefore, the resistive divider is required to restore every clock-period the correct value of the reference voltage at node $A$.

The limit is similar to the one already studied in Example 3.2. In this case the operation of the comparators is sampled-data and not continuous-time. Even here it is necessary to use a the references divider with a proper low value of unity resistance.

**Does Auto-zero Helps?**

The offset of a CMOS comparator can be reduced from some mV to fraction of mV. To be really effective auto-zero must be used in fully differential implementations.

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**Fig. 3.4 - Auto-zero techniques.**

![Auto-zero techniques diagram](image-url)
3.3.4 Practical Limits

The previous sub-sections showed that high-resolution and high conversion rates require very small resistances in the resistive divider. A side drawback associated to this request concerns the voltage generator used to feed the resistive string. The output impedance must be smaller than the impedance of the string itself up to the sampling frequency. An external reference requires a strong decoupling buffer to avoid ringing caused by the bonding inductance. Often, a band-gap reference is a low impedance internal buffer are preferred.

An *n*-bit full-flash architecture uses \(2^n\) comparators. Every increase by 1 bits doubles the system complexity. The exponential increase concerns both silicon area and, more important, power consumption. A practical upper limit to the power consumption establishes the maximum clock frequency and resolution. Consider, for example a full-flash converter running at 500 MS/s. A reasonable current for a comparator working at 500 MHz is 0.5 mA. Assume that the remaining part of the architecture consumes 50% of the comparators’ current. Thus, a 6-bit converter needs 96 mA. Comparators used for higher resolution will likely consume more current. However, even using the same current consumption, a 8-bit converter would need 0.4 A. With 2.2 V supply the power consumption would be close to 1 W.

The capacitance loading the input sample-and-hold is another important practical limit to speed and resolution. The capacitance of a single comparator is multiplied by the number of comparator. Thus, even if the comparator capacitance is very low, the capacitance loading the S&H becomes significant especially, for sustaining accuracies required by high resolution becomes. If the capacitance of a comparator is 40 fF the input load of an 8-bit flash is 12.8 pF, a very large value for a driver running at many hundred MHz.

The peak current at the output of the S&H is another limit. The S&H must be able to charge the load capacitance in a fraction, say \(\alpha\), of the sampling period, \(1/f_s\). If the largest input step is \(\Delta V_{in,max}\) the peak current of the S&H is

\[
I_{S&H,\, peak} = \frac{f_s C_{in} \Delta V_{in,\, max}}{\alpha}.
\]

For \(\Delta V_{in,max} = 1V\), \(C_{in}=12.8\, pF\), \(\alpha=0.1\) and \(f_s=250\, MHz\) \(I_{S&H,\, peak}=32\, mA\).

The limits discussed above make it unpractical an 8-bit full-flash with conversion speed higher than 500 MS/s. For 6-bit the upper limit is 2 GS/s.

**Use of Full-Flash**

Full-flash converters are suitable for high-speed but medium resolution. Practical limits make the technique unsuitable for more than 8-bit 500 MS/s.
3.4 SUBRANGING AND TWO-STEP CONVERTERS

The full-flash architecture is suitable for medium resolution. The exponential increase of silicon area, power consumption and the capacitive load of the S&H make the method unworkable above a given limit. An effective alternative to the full-flash technique is the sub-ranging or the two-step algorithm.

Fig. 3.5 shows the basic architecture. The input signal is sampled and held. An \( M \)-bit flash-converter estimates the MSB’s (coarse conversion). The DAC converts the \( M \)-bits back to analog. Then, the subtraction yields the quantization error (also called the residue) of the \( M \)-bit coarse quantizer. The second flash determines the LSB (fine conversion). Finally, the digital logic combines coarse and fine results to obtain the \( n = (M+N) \)-bit output. The gain stage is used only in a two-step architecture. If the gain equals \( 2^M \) the full scale of the residue equals the dynamic range of the first stage: the fine converter uses the same reference voltage of the coarse converter. By contrast; a sub-ranging scheme does not amplify the residue. The dynamic range of the residual is \( 2^M \) lower than the input and the second stage must use a scaled reference voltage.

Fig. 3.5 also shows the clocking scheme of the two-steps (or sub-ranging). The main clock generates four control signals: auto-zero and S&H, coarse conversion, DAC and residual generation and fine conversion plus. As a result, the entire conversion process requires two entire main clock periods.

Suppose \( M = N = 4 \). The comparators’ count is \( 2(2^4 - 1) = 30 \), much less than the \( (2^8 - 1) = 255 \) required by an 8-bit full-flash counterpart. Therefore, the chip area is much smaller; the power consumption and the S&H capacitive load decreases by a factor as large as \( 2^4 = 16 \).

![Fig. 3.5 - Block diagram of subranging (K=1) and two-step architectures (K>1).](image-url)
The obvious disadvantage of the method is a reduced conversion-rate: the algorithm requires two complete clock period to complete the conversion. However, the small capacitive load enables an higher speed in the S&H. Since the speed of the S&H is the full-flash bottleneck, using a S&H with enhanced speed partially compensates for the reduction of conversion-rate.

### 3.4.1 Accuracy requirements

The non-idealities of typical S&Hs don’t influence much low accuracy converters. When the resolution becomes medium-high as in a two-step architecture the performances of the S&H become important. Obvious limits of the S&H are offset and gain error. They cause an equal offset and gain errors in the ADC. The $kT/C$ noise of the S&H is also another potential limit. Its maximum permitted value is given by the quantization noise and the resulting $\text{SNR}=6.02(M+N)$ dB. We have seen in Chapter 1 that the power of the $kT/C$ must be well below the quantization noise power. This condition determines the value of the sampling capacitor. Finally it is necessary to ensure an S&H linearity at a level that meets the SFDR requirements.

Other blocks that influence the two-step converter performances are the coarse ADC and the DAC. These blocks determines the input to the fine ADC: an error on the residual causes an error on the LSBs that the fine ADC determine.

According to Fig. 3.5 the residual is

$$V_{\text{res}}(V_{in}) = K V_{in}; \quad \text{for } V_{ADC}(1) \leq V_{in}$$

$$V_{\text{res}}(V_{in}) = K [V_{in} - V_{DAC}(k)]; \quad \text{for } V_{ADC}(k-1) \leq V_{in} < V_{ADC}(k)$$

(3.15)

where $k$ is ADC output level described by to the $M$-bit code.

Ideal responses of coarse ADC and DAC make the amplitudes equal to $V_{FS}$ and 0 before and after the transition points. A non-ideal responses moves the transition points thus modifying the amplitudes at the breaks.

Let us focus before on the effect of coarse ADC non-ideality. Errors in threshold transitions, $\varepsilon_{ADC}(k)$, moves back and forth the breaks marking the the DAC subtraction. These errors change the residual only near the break transitions. Just before the break the error is $K \varepsilon_{ADC}(k)$. Since an ideal DAC leads to an exact subtraction the errors immediately after the break is exactly equal to error immediately before the break, $K \varepsilon_{ADC}(k)$.

Fig. 3.6 a) shows the effect of a possible real ADC. The transition between codes 000 and 001 occurs at an input voltage that is slightly higher than 0.125 (we assume $V_{FS} = 1$). Therefore, the first break occurs after the expected value; the residual amplitude continues to increase after 0.125 (see Fig. 3.6 b))
3.4. Subranging and Two-Step Converters

and exceeds $l$ in the interval $V_{in} = 0.125 + \varepsilon_{ADC(1)}$. At the break the error is $8\varepsilon_{ADC(1)}$. More in general, the value of the error is positive or negative as outlined by arrows but it occurs only in the small range around break points. In a large part of the input range the ideal and the real response are coincident.

The $ADC$ threshold inaccuracies depend on gain error, offset and $INL$. The $\varepsilon_{ADC(k)}$ is represented by

$$
\varepsilon_{ADC(k)} = V_{os} + \frac{V_{FS}}{2^M} \left\{ \varepsilon_{G,ADC} + INL_{ADC(k)} \right\}
$$

where $\varepsilon_{G,ADC}$ is the gain error; $INL_{ADC(k)}$ is measured in $LSB$.

We have seen that the effect of shifts in the $ADC$ threshold brings the residual beyond the limits $0$ and $1$ or the residual does not get the boundaries. In the first case the input to the fine $ADC$ is out-of-range. The output remains $0...00$ or $1...11$ until the input re-enters in the $0 - 1$ boundaries. If the residual does not get at $0$ or $1$ the fine converter does not start from $0...00$ or does not reach the full scale $1...11$.

We consider now the effect of a real $DAC$. Errors in the $DAC$ output modify the subtractive terms. Accounting for offset, gain error and the $INL$ the error is

$$
\varepsilon_{DAC(k)} = V_{os} + \frac{V_{FS}}{2^M} \left\{ \varepsilon_{G,DAC} + INL_{DAC(k)} \right\}
$$

Each $DAC$ error $\varepsilon_{DAC(k)}$ shifts up or down the residual in the range $V_{th,ADC(k)} ... V_{th,ADC(k+1)}$.

Fig. 3.7 a) shows a possible real $DAC$ response. At code $001$ the $DNL$ is positive (up arrow in Fig. 3.7 a). Thus, the shift down at the first break is larger...
than $I$ (down arrow in Fig. 3.7 b). The plot of Fig. 3.7 b) depicts the effect of the DAC error superposed to the one caused by the ADC. The horizontal arrows denote a shift in thresholds, the vertical arrows denote DNL error in the DAC. Observe that the error on the horizontal shift makes the real transfer characteristic different from the ideal one in the entire coarse quantization interval. Thus, the accuracy request for the DAC will be more demanding than for the ADC.

Fig. 3.8 shows four possible situations. The fine conversion uses 4-bit. The case a) is ideal. The residual switches from $V_{FS}$ to 0 when an MSB transition occurs. Before the transition the fine ADC determines 1111 and after 0000. In case b) the residual exceeds the limits on both sides. The output of the fine ADC remains on the 1111 and 0000 levels for an input range larger than one LSB. The case c) shows what happens when the residual does not reach 0 after

Fig. 3.8 - Residual plots around a break point and the generated transfer characteristics.
the break. The fine quantization immediately after the break gives 0010; the codes 0000 and 0001 are missing. The case d) shows the case of another missing code (1111) before the MSB transition.

Fig. 3.9 shows the static response in three different cases: ideal response, with real ADC and ideal DAC, and with both ADC and DAC real. Observe that errors for the second case appear only around the MSB transitions. Far away 1 or 2 LSB the response follows the interpolating line. In the third case the shift error due to the DAC brings the response above or below the interpolating line.

**Example 3.5**

Study with computer simulations the behavior of a two-step 4+4 bit converter. Model the transfer characteristics of ADCs and DAC with a random DNL and include distortion terms up to the fifth order. With a full-scale sine wave determine output spectrum and equivalent number of bit. Determine the effect on output spectrum of ADC and DAC non-idealities.

**Solution:** The file statchar.m generates the static characteristic. The analog range (firstbin - lastbin) is divided into nbin-1 intervals. The ideal response is calculated. Then, offset and a random
term representing the DNL are added to the ideal response. The file dist.m distorts the static response. The distortion terms do not modify the values at the ending points. The file Ex3_5.m simulates both a full-flash and a two_step architecture. A flag permits the user to make the choice. The input signal is a linear ramp (to plot the transfer characteristic) or a sine wave. Even in this case a flag enables the selection. Fig. Ex. 3.5 show the output spectrum for $f_s/f_{in}=35.31$. The left side plot depicts the ideal case. The SNR is 49.9 dB corresponding to 8 bit. The right side spectrum accounts for a random DNL which maximum is 0.5 LSB and a 0.01 third order distortion coefficient. Equal non-idealities affect ADCs and DAC. The tones on the spectrum cause 47.2 sB SFDR. 0.5 bit is lost because of the random DNL. The use of the provided files permits a more extensive study of limitations and features.

3.4.2 Two-step Conversion as a Non-linear Process

The residual generator output of a two-step converter is the quantization error of the coarse ADC. Observe that generating the residual is equivalent to a non-linear transformation of the input. Fig. 3.10 shows the non-linear response. The transfer curve is non-univocal: it maps many inputs with single outputs. Moreover, the input-output relationship is linear in sections where the slopes are equal. The amplification block models the possible interstage gain. The non-linear generation of the residual is also described by equations. They are given on the right side of Fig. 3.10.

The digital code that denotes the residual represents many input levels. The
3.5 Folding Technique

A data converter distinguishes between many inputs by using the digital code given by the coarse ADC.

The above description is not only a repeated explanation of the two-step or the subranging algorithm but it is also a useful outline of the input-residual relationship. The non-linearity feature is important: a linear block possibly modifies amplitude and phase of the composing input frequencies but it does not generate new spectral terms: a band-limited input remains band-limited. By contrast, a non-linear transformation generates new spectral terms. Thus, a band-limited input that occupies a fraction of the Nyquist interval leads to a residual which spectrum spans over the entire Nyquist range. The result does not violate the Nyquist theorem: the signal is already in the sampled data domain. However, the speed of the circuit generating the residual becomes critical. Analog subtractor and interstage amplifier must be fully performant up to the Nyquist limit, $f_s/2$.

A possible distortion in the linear sections of the residual influences the global harmonic distortion in a limited manner. An intuitive explanation comes for observing that the residual is not correlated (or has a very limited correlation) with the input. The effect of a possible distortion should be referred to the input and the result is almost noise. For this reason the linearity of the residual generator is not a critical factor. The SNDR and the SFDR are mainly controlled by the non-linearities of the first ADC and the DAC.

3.5 Folding Technique

We have seen that the residual is a non-linear transformation of the input. The main feature is that the response is linear in various sections that divide the input dynamic range. Other possible non-linear responses with an equivalent feature are the ones of Fig. 3.11. The response of Fig. 3.11 a) divide the input into 4 sections. Fig. 3.11 b) identifies eight input sections. The responses are linear inside each sector but the slope alternates between $+1$ and $-1$. The non-linear responses can be viewed as the multiple folding of a linear ramp (two
times and four times folding respectively). Thus, the name to the techniques comes from the specific analog pre-processing of the input.

**REMEMBER THAT**

The input to a folder is band-limited but the spectrum of the output is spread over the entire Nyquist interval.

The antialiasing filter must be placed before the folder and not after!

A single folding bends down an input ramp around 1/2 \(V_{FS}\). Folding is represented by one bit. The peak value is 1/2 \(V_{FS}\). Folding twice (two bits) leads to a peak value equal to 1/4 \(V_{FS}\). Folding three times (three bits) leads to 1/8 \(V_{FS}\) peak value and so forth. The peak amplitude after \(M\)-bit folding becomes \(1/2^M\). Since folding diminishes the dynamic range, the number of quantization intervals for achieving a given resolution diminishes accordingly. Thus, using an \(M\)-bit folder reduces the number of quantization intervals of an \(n\)-bit converter down to \(2^n/2^M\). Knowing the segment containing the input generates the MSBs. Quantization of the folded result gives the LSBs.

Fig. 3.12 depicts a conceptual architecture for a folding converter. An \(M\)-bit folder produces two signal: the folded output and an \(M\)-bit word coding the input. The input to a folder is band-limited but the spectrum of the output is spread over the entire Nyquist interval. The antialiasing filter must be placed before the folder and not after!
segments containing the input. The gain stage augments the dynamic range of the folded signal to \( V_{FS} \); the \( N \)-bit ADC determines the LSBs. The digital logic combines the data and generates the \( n = (N+M) \) bit output.

The accuracy of the folding converters depends on the accuracy and the linearity the folder. Limits to linearity are both static and dynamic. We will see that the circuit implementations use current switching or employ the voltage-to-differential current relationship of MOS transistor pairs. In both cases the slope transition at the folding points is not sharp. The response is somewhat rounded. Also, at high frequency the parasitic capacitances in the folder and the associated resistances establish limiting time constants. The non-linear response of the folder changes with respect to the static response. The result depends in a complex way by the time constants of the folding network.

### 3.5.1 Double Folding

The response of a folder is typically linear midway the folding points. The non-linearity increases when approaching the transition regions and results into a rounding of the transfer curve at the folding points. The conveyed non-linearity affects the input of the fine converter.

Often the rounded regions are too wide for the required linearity. However, outside those critical ranges the situation is acceptable. Thus, for a given linearity we can identify intervals of the folded curve that permit complying the specifications and other regions that are not acceptable. Fig. 3.13 (top) shows the
possible folding response of a real circuit. The regions whose linearity com-
plies the specifications are marked with \( G \) (good) the other are marked with \( B \)
(bad).

A method to dischard the bad regions and work only in the good regions
employs t\(w \)e folders. The transfer characteristics are shifted one with respect
to the other by a quarter of folding period. Thus on folder is in the linear
region when the other is the bad region. For any input voltage there is a linear
region that the system can utilize. Two folders require two fine flash-conver-
ters. However, the dynamic range used by each the convert is a fraction of the
folded outpot (thick lines in Fig. 3.13). As a result the number of comparators
necessary for the flashes equals to one of a single-folder system (practical rea-
sons may require overlapping the converters range a bit beyond the half
range).

## 3.6 INTERPOLATION

Interpolation is the generation of an electrical variable that is intermediate
between two other electrical variable. Interpolation is normally achieved by
resistive or capacitive dividers. Consider for example the simple circuit of

![Fig. 3.14](image)

Fig. 3.14 - Simple circuits that acheve the interpolation of two voltages.

Fig. 3.14 a). The voltage \( V_{\text{inter}} \) is given by

\[
V_{\text{inter}} = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}.
\]  

(3.18)

The circuit of Fig. 3.14 b) accomplishes interpolation with capacitors. \( C_1 \)
and \( C_2 \) are dischraged during phase \( \Phi_1 \) and generate the output voltage during
the complementary phase, \( \Phi_2 \).
3.6. Interpolation

The discharging phase remove residual charges that possibly affect the initial conditions. Since the operation of the capacitive interpolator is sampled-data it can be used only in circuits that permit a reset period.

Assume $V_1$ and $V_2$ the output of two gain stages with equal gain $G$ (Fig. 3.14c) whose inputs are $V_{in} - V_{refA}$ and $V_{in} - V_{refB}$ (Fig. 3.14c).

\begin{equation}
V_1 = G(V_{in} - V_{refA}); \quad V_2 = G(V_{in} - V_{refB}).
\end{equation}

The interpolation of $V_1$ and $V_2$ with two equal resistors $R_1 = R_2$ leads to

\begin{equation}
V_{\text{inter}} = G\left(V_{in} - \frac{V_{refA} + V_{refB}}{2}\right)
\end{equation}

showing that interpolation equals the use of an extra gain stage amplifying $V_{in} - (V_{refA} + V_{refB})$. The result is interesting: two equal resistors replaces the function of an intermediate gain stage.

### 3.6.1 Use of Interpolation in Flash Converters

Often flash converters use interpolation. Fig. 3.15 describes the method. The architecture of a sampled-data comparator is made by a preamplifier and a latch. The output of each gain stage is the differential input amplified for a given input range. Then, the output saturates at an upper or a lower clipping levels near the supply voltages. The swing that brings the output from the lower to the upper saturation is normally larger than $V_{ref(i)} - V_{ref(i-1)}$. Therefore, as shown in Fig. 3.15 b), the two successive preamplifier have an overlapped regions where the responses are non-saturated. The use of the interpolation network generates responses with zero crossing midway between the zero crossing of the preamplifiers. At the zero crossings the slope is the same of the generating curves. Only at the top and bottom the slope is smoother. However, this is irrelevant for the following use: the voltages drive a latch.

For a given resolution the flash uses the same number of latches but the preamplifiers and reference voltages are halved. Therefore, the capacitive load on $S&H$ and the resistors of the references generator are divided by two.

Some architectures use the preamplifier used before the latch made by two gain stage. In this case it is possible to use interpolation after the first and the second gain stage. Therefore the benefit on $S&H$ parasitic capacitance and number of reference voltages becomes four.

The method described in Fig. 3.15 can be extended to multiple interpolation:
the series connection of many equal resistors between preamplifers provide multiple controls for latches. The number of preamplifiers and reference voltages are reduced by a factor equal to the number of resistors used.

Interpolating networks can also operate with ully differential preamplifier driving latches with differential inputs. Another possibility is using capacitive interpolators instead of resistive dividers.

### 3.6.2 Use of Interpolation in Folding Architectures

The interpolation technique can also be used in folding architectures. In some case an extensive use of interpolation replaces the fine flash converter. Fig. 3.15 a) shows the interpolation of two folding responses, $V_{F1}$ and $V_{F2}$, shifted by half a segment. The shape of the interpolation curve is more rounded than the generating terms (actually it is almost flat). However, the zero crossings are midway two consecutive zero crossings of the generating curves. Interpolating $V_{F1}$ and $-V_{F2}$ as shown in Fig. 3.16 b) produces the other midway zero crossings. Thus, the number of zero crossing can be doubled.
The use of not equal resistances in the interpolator produces additional zero crossings. For example, as shown in Fig. 3.16 c), an interpolating divider made by \( R_1 = 3R_2 \) produces zero crossings at \( 1/4 \) from the zero crossing of \( V_{F2} \). Using multiple interpolations with \( V_{F1} \) and \( V_{F2} \) or their inverse generates a number of zero crossing that can be large enough for the LSB determination. Therefore, the fine flash converter can be replaced by just a set of comparators capable to determine the zero crossing of interpolated signals.

### 3.6.3 Use of Interpolation for Improving Linearity

The interpolation method is used to average static errors (like the mismatch in the offset of preamplifiers or the error in reference voltages). Consider again the circuit of Fig. 3.15. If the output resistance of the preamplifiers, \( R_{out} \), is much smaller than the resistances in the interpolating network, \( R_{inter} \), the circuit works as already studied. If \( R_{out} \) is comparable or larger than \( R_{inter} \) neigh-

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**USEFUL FEATURE**

Interpolation can be at any position: the use of suitably ratioed resistors procures zero crossings located anywhere among zero crossings of interpolating curves.
bor preamplifiers interfere one each other thus affecting the output of preamplifiers and interpolated values. The preamplifier outputs change even for error free conditions. However, if the input of a given preamplifier is zero the interpolation network does not affect the output that remains zero: the push of preamplifiers on the bottom is balanced by an equal pull of preamplifiers on the top.

The interpolating network smooths possible errors on the preamplifier outputs. Fig. 3.17 gives a simple model for studying this feature. Assume that the input of the middle preamplifier (the \( i \)-th) is zero. Its voltage source is just the error, \( \varepsilon_i \). The outputs of the preamplifier one level up and one level down are \( G \cdot \Delta + \varepsilon_{i+1} \) and \( -G \cdot \Delta + \varepsilon_{i+1} \) respectively, the ones two levels far away generate \( G \cdot 2 \Delta + \varepsilon_{i+2} \) and \( -G \cdot 2 \Delta + \varepsilon_{i-2} \) and so for until the saturation clips the output voltages to \( V_{\text{sat}+} \) and \( V_{\text{sat}-} \).

The reference voltage that is relevant for the data converter is the one establishing the crossing, \( V_{\text{out}}(i) \). The error on \( V_{\text{out}}(i) \) is given by the superposition of the effect of errors affecting all the source generators of Fig. 3.17

\[
V_{\text{out}}(i) = \sum_{j=1}^{K} G(E_j + \varepsilon_j)T_{i,j}
\]

(3.22)

where \( E_j = 0 \), \( K \) is the number of preamplifiers, and \( T_{i,j} \) is the attenuation at output \( i \) for a source generator at \( j \). The attenuation factor \( T_{i,j} \) diminishes with \( |i-j| \) and, in practical cases, it is very small for \( |i-j| = d > 4 \). Moreover, the attenuation coefficients sums up to \( I \).

Accounting for errors only, after interpolation, the error is
3.6. Interpolation

Stating that the error at the comparator with zero input is the weighted sum of errors of \((2d+1)\) neighbors. The weighted sum smooths the short distance non-idealities thus reducing, as expected, the DNL.

**Example 3.6**

Estimate with Spice simulations the improvement of the DNL due to an interpolating network connecting 63 preamplifiers. The value of the interpolating resistance equals the preamplifier output resistance. Use the equivalent circuit of Fig. 3.17. Estimate the attenuation factors considering only \(5+5\) neighbours.

**Solution:** The equivalent circuit of Fig. 3.17 with 11 cells makes the Spice test circuit. For the simulation we the input voltages of Fig. Ex 3.6 a). The same figure gives the output. The output is spreaded out just a little with respect to the input. For example, the output of preamplifier \#8 is 0.706 while the input is 0.85. The input of the preamplifier \#6 is zero. The output, as expected, is zero. Simulations with just one source equal to 1 determine the attenuation factors. The results are: \(T_{\delta,6}=0.44; T_{\delta,5}=T_{\delta,7}=0.17; T_{\delta,4}=T_{\delta,8}=0.06; T_{\delta,3}=T_{\delta,9}=0.02; T_{\delta,2}=T_{\delta,10}=0.01\). Observe that the last two attenuation factors are so small to make negligible the contributions of the \(\pm3\) and \(\pm4\) neighbours.

A random signal models the DNL. Random numbers applied to a spatial filter with coefficients given above give the results of Fig. Ex 3.6 b). The spatial filter operates well on short distance varia-

\[
\varepsilon_{\text{inter}}(i) = \sum_{j = i - d}^{i + d} G \cdot \varepsilon_j T_{i,j}
\] (3.23)
3.7 TIME-INTERLEAVED CONVERTERS

The interleave method enables increasing the conversion rate of a data converter [11]. The approach uses a number of converters working in parallel with interleaved sampling times. The combined action of the converters is equivalent to a single converter operating at a multiple of the sampling rate of a single data converter. Fig. 3.18 illustrates the basic concept. The input sample-and-hold runs at $f_s$ and acquires the signal to be converted. An analog demultiplexer provides the inputs to $N$ parallel ADCs whose sampling frequency is $N$ times lower than the overall sampling rate, $f_s$. The samples are thus processed by the cooperative proceeding of equal ADCs. The digital multiplexer sequentially selects the output of various channels and forms an high-speed ADC.

Increasing the throughput is an interesting feature. However, the performance of time-interleaved architectures is sensitive to the mismatch among various ADC used in channels [12]. Offset, gain, and sample-time mismatches between channels are the most relevant sources of error.

We estimate the limits by considering the sources separately. The first examines is the offset. If all the ADCs have the same offset the result is just a global shift of the output. By constrast, if only one channel is affected by off-

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Fig. Ex. 3.6 b) - Smoothing action of the interpolation on a possible DNL.
3.7. Time-Interleaved Converters © F. Maloberti

set, the error will appear at the output every $N$ clock periods. The result is a pulse at $f_s/N$ superposed to the output. More in general, offset mismatches will cause a periodic additive pattern at $f_s/N$. Since Nyquist is at $f_s/2$, the spectral components of the additive pattern falls inside the Nyquist interval.

The requested SFDR establishes an upper limit to the offset mismatch. The worst case is when offset changes like a sine wave along the interleaved elements. The additive pattern is a sine wave which amplitude is half the peak-to-peak offset mismatch, $\delta V_{os}$. The Fourier spectrum is a contains a line which amplitude is $\delta V_{os}/2$. The limit to offset mismatch becomes

$$\delta V_{os} < \frac{1}{2} \cdot V_{FS} \cdot 10^{-SFDR/20}. \quad (3.24)$$

Using an SFDR equal to the SNR the maximum permitted offset mismatch is $0.5$ LSB. The condition is difficult to fulfill for more than 10 bit ($0.5$ LSB is $0.1 \text{ mV}$ or less). Moreover, offset, that is often an irrelevant limit to high-speed applications, becomes a critical design parameter.

Let us consider now the gain error. A uniform error is not a problem. The same limit affects the time-interleaved converter. Instead, a gain mismatch between channels causes an amplitude of the input modulation by the periodic sequence of channel gain. A full amplitude sine wave with amplitude $A_{in}$ and frequency $f_{in}$ modulated by a sine-wave shaped gain sequence gives

---

Fig. 3.18 - Time-interleaved architecture.
where $\varepsilon_G$ is the peak gain mismatch. The amplitude of the modulation products is $A_{in} \varepsilon_G/2$. Therefore, the SFDR is $\varepsilon_G/2$.

The $SDNR$ deteriorates because of the power of the modulating terms. Assume a request of $SDNR$ just $1\, \text{dB}$ less than the $SNR$. With full scale input the power of modulating spur must be a quarter the quantization noise. The condition

\begin{equation}
2 \left( \frac{V_{FS}^2 \cdot \varepsilon_G^2}{32} \right) = \frac{1}{4} \left( \frac{V_{FS}^2}{12 \cdot 2^{N\text{bit}}} \right)
\end{equation}

leads to

\begin{equation}
\varepsilon_{G, \text{pp}} = \frac{1}{2 \sqrt{3}} \cdot \frac{1}{2^{N\text{bit}}} = 0.29 \cdot \frac{1}{2^{N\text{bit}}}
\end{equation}

Thus, for $10\,-\text{bit}$ the peak-to-peak gain error, $\varepsilon_{G, \text{pp}}$, must be 0.29%. The control of the gain error at this level of accuracy is very difficult. Only complex calibration schemes (studied in a successive Chapter) achieve the goal [13].

The scheme of Fig. 3.18 uses an input high-speed $S\&H$. The solution is optimal for uniform sampling but the design of a very-high speed $S\&H$ is problematic. A more affordable solution foresees one $S\&H$ per channel and time-interleaved sampling clocks. The circuit design is smooth but the random systematic delays of the sampling instants introduce errors.

If the input is a sine wave, $V_{in} = A_{in} \sin(\omega_{in} t)$, a mismatch by $\delta t$ of the $S\&H$ sampling time gives

\begin{equation}
V_{in}(nT + \delta t) = A_{in} \sin(\omega_{in}(nT + \delta t)) - A_{in} \omega_{in} \delta t \cos(\omega_{in} NT)
\end{equation}

where the sampling mismatch, $\delta t$, is assumed much smaller than $T$.

Assume the clock error delay of channel $n$ $\delta t_n = 0.5 \, \delta t_{\text{max}} \sin(2\pi n/N)$. The second term of equation (3.28) leads to two modulation products whose amplitude is $A_{in} \pi f_{in} \delta t_{\text{max}}/2$. If we want that the power of the modulation terms is a quarter the quantization power, with full scale input and frequency at

\begin{equation}
V_{out}(nT) = A_{in} \sin(2\pi f_{in} nT) \cdot \left[ 1 + \varepsilon_G \sin\left( \frac{2\pi n}{N} \right) \right]
\end{equation}
Nyquist ($f_{Nyquist} = 1/2T_s$) it is necessary to have

$$\delta t_{peak} = \frac{1}{\sqrt{3}\pi} \cdot \frac{T_s}{2^{N_{bit}}} = 0.184 \cdot \frac{T_s}{2^{N_{bit}}}.$$  \hspace{1cm} (3.29)

Thus, a 2-channel time-interleave 10-bit converter running at 200 MS/s (the channel clock is 100MS/s) requires a clock distribution with delay mismatch lower than 0.72 psec.

**Example 3.7**

A four channel time-interleaved uses 12-bit 65 MHz ADCs in each channel ($V_{FS} = 2V$). The required SFDR is 80 dB with -20 dBFS input. Estimate offset, gain and sampling time mismatches.

**Solution:** The offset mismatch determines a spur line with amplitude $\delta V_{os}/2$. It must be 80 dB below the -20 dBFS input. Therefore, the peak-to-peak offset must be -94 dBFS. $V_{FS} = 2V$; $\delta V_{os} = 40 \mu V$.

The amplitude of the spur caused by gain mismatch is $A_{in} f_{G,pp}/4$. The amplitude of the spur caused by sampling-time mismatch is $A_{in} \pi f_{in} \Delta t_{pp}/4$. The sampling frequency of the overall system is 260 MHz. Nyquist is 130 MHz. Both gain error and sampling-time error must be 80 dB below $A_{in}$. Therefore

$$e_{G,pp} = 4 \cdot 10^{-4}; \quad \delta t_{pp} = \frac{4}{\pi} \cdot 2T_s \cdot 10^{-4} = 0.97 \text{ ps}.$$  

**3.8 SUCCESSIVE APPROXIMATION CONVERTERS**

One goal of the algorithms studied in previous sections is to procure a high conversion speed. All the methods accomplish the conversion in a small number of clock periods; for the time-interleave technique the conversion in each path can require many clock periods but the cooperative action of the converters increases the overall throughput.

The main objective of the successive approximation algorithm is not to achieve an high conversion rate but it is rather for minimizing the circuit complexity and reducing the power consumption. Fig. 3.19 helps in describing the method. The figure refers to a 3-bit ADC but can be extended to any number of bits. The dynamic range $0 - V_{FS}$ is divided into 8 quantization intervals. The first clock period enables sampling and holding of the input. Assume, as shown in the figure that after a transient $V_{S&H}$ settles at a given level inside the 101
interval. The next clock cycle determines the MSB. We known that the MSB is 1 if the input is larger than $V_{FS}/2$ and 0 otherwise. The MSB value results by comparing the input with the output of a 3-bit DAC generating $V_{FS}/2$. If the MSB is 1 the next bit is 1 or 0 if the input is larger or smaller than $3V_{FS}/4$. If the MSB is 0 the level to consider is $V_{FS}/4$. Thus, the value of the already determined MSB determines the proper value of the next threshold voltage. The MSB and the next bit set the new comparison level ($6V_{FS}/8$ in the figure) for determining the LSB. The method illustrated in Fig. 3.19 requires a 3-bit DAC to generate the successive threshold voltages. To extended the method to more bits it is necessary to use more periods and a DAC with proper resolution.

The method requires one clock period for S&H and one clock period for each bit. Thus, an N-bit converter needs $(N+1)$ clock intervals. In some cases a precise S&H can need a time that is higher than the one required by bit estimation. To avoid the bottleneck of the S&H speed two clock period instead of one can be used for the S&H. The conversion time becomes $(N+2)$ but the usable clock frequency is higher than the one with $(N+1)$ timeslots.

Fig. 3.20 shows a diagram implementing the successive approximation algorithm. The S&H samples the input during the first clock period and holds it for $N$ successive clock periods. The digital logic controls the DAC according to successive approximation algorithm; it is named successive approximation register (SAR). At the beginning of the conversion the MSB is set to 1. It is a guessing of the MSB value. If the comparator confirms the guessed the value it is retained, otherwhise the MSB is changed to zero. The next clock period the next bit is temporarily set to 1. The comparator confirms or not this prediction and after confirmation the algorithm proceeds in the same way until the LSB. The logic provides the output while the S&H samples the next input.
The voltage $V_{DAC}$ changes at the rising edge of $\Phi_{DAC}$ and remains available for an entire clock period. The control by the SAR is such that $V_{DAC}$ tracks $V_{S&H}$ thus establishing a search path. Fig. 3.21 a) shows a possible search path for $V_{S&H}$ equal to $0.364V_{FS}$. The distance between $V_{DAC}$ and $V_{S&H}$ decreases as the algorithm progresses and the error is less than successive divisions by two of $V_{FS}$. However, an error of the comparator output at a given changes the search path and the error propagates along all the successive steps. Assume, as shown in Fig. 3.21, that $V_{DAC}$ changes from a level well below $V_{S&H}$ to a level just above (fourth slot). The recovery of the comparator from overdrive can not be fast enough and eventually the comparator determines a 1 instead of a 0. The next $V_{DAC}$ voltage brings the search path in a wrong direction and the following search path becomes 0000. The correct con-

![Fig. 3.20 - Basic circuit diagram fo the successive approximation algorithm.](image)

**COMPARATOR ERROR**

A comparator error at any point of the search path can not be recovered and affects the remaining part of the algorithm.

![Fig. 3.21 - Errors in the successive approximation search.](image)
version gives 1110. The error at the end of the conversion is 2 LSB.

The accuracy of successive approximation converters also depends on accuracy of S&H and DAC. The errors of the two blocks are superposed and can be referred to the input. They lead to random and distortion terms affecting the DNL and the INL.

**Example 3.8**

Simulate the static behavior of an 8-bit successive approximation converter. Use a slow ramp at the input and estimate INL and INL. Model the response of the DAC using a second and a third harmonic distortion term.

**Solution:** A slow ramp starting from 0 that achieves the full scale in $K \cdot 2^8$ sampling periods permits to acquire of $K \cdot 2^8$ points. If the response is ideal each bin will contain $K$ samples. In such a case the histogram of the set of data is flat. The non-ideality of the DAC modifies the histogram. If the quantization interval is smaller than the ideal value the bin will contain less samples. The contrary if the quantization interval is bigger than the ideal value. The histogram enables the DNL and the INL estimation. Since each bin contains an average of $K$ samples the accuracy of the DNL estimation will be $1/K$.

The Matlab file Ex3_8_SAR.m provides the basis for solving the problem. The file SuccAppr.m implements the algorithm. The simulation uses 12800 points. Accordingly, the simulation brings an

![Fig. Ex. 3.8 a)- DNL (the resolution is 0.02).](image)
average of 50 samples per bin. The DNL accuracy is 0.02 LSB.
The input signal is a ramp with superposed a small (0.001 peak-to-
peak) noise. The effect of the noise slightly randomizes the DNL.
The INL is the running sum of the DNL; this averaging action
makes irrelevant the effect of the noise on the INL.
The use of the function dist.m produces the second (0.005) and the
third (0.005) harmonic distortion terms. The plot of Fig. Ex. 3.8 b
shows that the given distortion terms bring about a maximum 0.85
LSB INL.

3.9 PIPELINE CONVERTERS

Pipelining is the parallel execution of any data converter sequential algo-
rithm: multiple stages perform at the same time the sequence of operations
required by the algorithm.

An example of sequential algorithm is given by the two-step technique. The
two-step converter uses two clock periods for determining sequentially MSBs
and LSBs. The pipelined version of a two-step achieves MSBs and LSBs at the
same time: while the coarse flash calculates the MSBs of one sample, the resid-
ual generator develops the quantization error of the previous sample enabling
the fine flash to produce the LSBs of that previous sample. The method
improves the throughput at the cost of latency time.
Another algorithms suitable for pipelining is the successive approximation. Its pipelined version obtains the conversion by unfolding the loop of Fig. 3.20 upon successive stages. Each stage estimates one bit. Hence, for \( n \)-bit it is necessary to use \( n \) stages. Other pipeline architectures blend two-step and successive approximation methods: they use three or more stages with single or multiple bits per stage. If the number of bits in the \( i \)-th stage is \( n_i \) and stages are \( k \) the total resolution becomes

\[
n = \sum_{i=1}^{k} n_i
\]

The block diagram of a generic pipeline architecture is shown in Fig. 3.22. The first stage determines one or more MSB bits \( \{b\}_1 \); the next stage decides additional bit(s) \( \{b\}_2 \) and so forth until the last stage that estimates the LSBs \( \{b\}_k \). Each stage generates a digital output and the residual used as analog input of the next stage. Assume that each stage uses the first half-clock period for the sampling and the bit evaluation; the second half is for the residual generation. The timing of the next stage must synchronize input sampling with residual availability. Using alternatively clock and its inverse along the pipeline chain ensure the synchronization. As already mentioned, sampling rate and output rate are at the clock frequency.

The bits generated by the second stage are delayed half a clock period with respect to the bits at the output of the first stage. The same is for successive stages. The digital logic must combine the bits using proper delay lines to produce the global digital output. Fig. 3.23 illustrates the timing for a 10-bit, 2-bit-per-stage pipeline. The bits \( b_9 \) and \( b_8 \) of the \( n \)-th sample are at the output of the first stage at time slot \( n+1 \). Bits \( b_7 \) and \( b_6 \) are generated at time \( n+2 \) by the second stage. The LSBs \( b_3 \) and \( b_0 \) are generated at time \( n+5 \). The combination of data is ready at time \( n+6 \). Fig. 3.23 also features the pipeline operation: at time \( n+4 \) while the stage 4 generated bits \( b_3 \) and \( b_2 \) of the \( n \)-th sample, stage 3
generates the bits \( b_5 \) and \( b_4 \) of the \((n+1)\)-th sample.

Fig. 3.24 is the block diagram of a generic pipeline stage. The ADC generates \( j \)-bits. The DAC has the same number of bits. The voltage However, as we will study shortly, architectures with digital correction use a resolution in the DAC lower than the resolution of the ADC. The subtraction of the DAC output from \( V_{in} \) gives the quantization error of \( V_{in} \) quantized with the number of bits of the DAC. The residual voltage at the generic \( j \)-th stage is given by

\[
V_{res,j} = (V_{in,j} - V_{DAC}\{b\}_j) \cdot K_j
\]

(3.31)

where \( K_j \) is the interstage gain. The amplification given by the interstage block augment the dynamic range of the residual. If the number of bits of the DAC is \( n_j \) and the gain is \( K_j = 2^{n_j} \) the dynamic range of the residual equals the dynamic range of the input. This condition permits the designer to use in all the pipeline state the same reference voltage.

Fig. 3.24 - Block diagram of a pipeline stage.
Fig. 3.25 shows input output transfer characteristics of the residual generator. The input ranges from $-V_R$ and $V_R$. For 1-bit ADC (Fig. 3.25 a) the output is 1 for positive inputs and 0 for negative inputs. The output of the DAC is $\pm VR/2$ (distance between the midway point of the bins) and $K=2$. If the input is just below 0 the residual is $V_R$; if the input is just above 0 the residual jumps to $-V_R$. At the lower and upper limits of the input dynamic range the residual is $-V_R$ and $V_R$ respectively. For a 3-bit ADC, 3-bit DAC, and $K=8$ we obtain the response shown in Fig. 3.25 b). The plot shows 7 breaks corresponding to the 7 transitions between the 8 quantization intervals of the DAC. The gain is $8=2^3$ and the dynamic range of the residual is again $\pm V_R$.

### 3.9.1 Accuracy Requirements

The number of bits that must be estimated decreases when moving along the pipeline architecture. If the interstage gain maintains constant the dynamic range of residual, accuracy requirements diminish throughout the structure. Therefore, design difficulties mainly regard the first few stages of the pipeline including, obviously, the input S&H.

Offset, gain error and linearity of the input S&H are translated into offset, gain error and distortion of the entire pipeline ADC. Non idealities of the ADC, DAC and residual generators affect the DNL and the INL. They have been already discussed for the two-step architecture. Similar limitations apply for the pipeline.

**Observation**

The non-linear response of the residual generators spreads the input spectrum over the Nyquist interval. The operation of the digital logic “rebuilt” the input spectrum.
We know that errors affecting the ADC lead to a shift of the break points in the residual response. Also, around the break points the amplitude of the residual exceeds the positive or the negative full-scale. Fig. 3.26 shows a residual response with real ADC and ideal DAC and interstage amplifier. The input range is $\pm V_{\text{ref}}$ and the interstage gain is $2^{N_{\text{bit}}}$. The top figure refers to a 1-bit per stage architecture. A possible ADC error moves the break point from zero to a positive value: the residual exceeds $V_{\text{ref}}$ in the input interval $0 - \text{break point}$.

Since $\pm V_{\text{ref}}$ is the dynamic range of the next stage an error occurs when the input exceeds the range. For 3-bits (Fig. 3.26, bottom response) the situation is similar. The number of input intervals that possibly cause errors equals the number of break points (7 for 3-bit).

Note that the error occurs because the next stage clips the residual and not because the residual value exceeds the bounds: the “information” carried by residual is preserved until clipping. Avoiding clipping is the first step for correcting ADC limitations.

### 3.9.2 Digital correction

The digital correction technique is used to compensate for the ADC non-ideality. The method can be used in pipeline architectures with any number of bits per stage. The technique is described before for a 1-bit per stage scheme; then the method is extended to multi-bit architectures. Fig. 3.26 supports the description. The basic feature of the digital correction technique is that the ADC provides redundancy. For 1-bit two threshold levels instead of one are used. The two thresholds are nominally symmetrical with respect to the zero input. The input range is divided into three regions. One is before the lower threshold, one is across zero, and the last one is after the upper threshold.

If the limits $V_{\text{th, L}}$ and $V_{\text{th, H}}$ are large enough even in presence of a plausible
error the input is certainly negative below the lower threshold and is certainly

positive above the upper threshold. In the median region the input is positive or negative but its amplitude is small. Thus, the value of thresholds establishes an interval of uncertainty where possible errors cause an incorrect bit estimation.

The output of the DAC depends on which region includes the input. The generated voltage is $-V_{ref}/2$ for 0 logic and $+V_{ref}/2$ for 1 logic. In the grey interval the output of the DAC is 0. Thus, the residual in the uncertain range is simply the amplification by 2 of the input.

We know that a 1-bit ADC distinguishes between two intervals, a 2-bit ADC differentiates four intervals. The above method used three intervals. Midway between the 1-bit and the 2-bit levels. This feature is normally expressed by saying that the resolution is 1.5-bit.

Fig. 3.27 shows the residual obtained by using a 1-bit and 1.5-bit DAC. Fig. 3.27 a) refers to ideal cases. Both transfer characteristics start at $-V_{ref}$. When $V_{in}$ equals $-V_{th,L}$ a first break in the 1.5-bit response occurs. The residual voltage just before the break is $V_{ref}-2V_{th,L}$. Immediately after the break it is $-2V_{th,L}$. Then, the residual is again a straight line with slope 2. The line crosses the 0 - 0 point. Observe that if $V_{ref} = V_{th,L}$, the swing of the residual around the break is symmetrical with respect to zero. At $V_{in} = V_{th,H}$ we have a second break and the residual response jumps down from $2V_{th,H}$ to $-V_{ref}+2V_{th,H}$. After the second discontinuity the residual is again a straight line with slope 2. The residual for the 1-bit response has a only one break for zero input. The residual value changes from $+V_{ref}$ to $-V_{ref}$.

**NOTE**

Digital correction compensates for ADC error only. Errors of DAC and residual generator don't improve with digital correction.
Fig. 3.27 b) shows the plots with errors in the ADC. A $\delta_{th}$ error in the threshold of the 1-bit ADC makes the residual bigger than $V_{ref}$ in the region $0-\delta_{th}$. For 1.5-bit an error $\delta_{th,L}$ in the first threshold of the ADC anticipates the break. The residual value at the break point is not $V_{ref} - 2V_{th,L}$. The value is $V_{ref} - 2(V_{th,L} + \delta_{th,L})$. Moreover, after the break we have $-2(V_{th,L} + \delta_{th,L})$. Both values are not correct but the plot is well inside the bounds. The same happens at the second break point. The result is that the input intervals that surely identifies a logic 1 or 0 are different from the ideal case. The range of the grey region is also different. However, the residual is within the bounds and no information is lost. The task of determining the bit is transferred to the next stage as it happens for the ideal 1.5-bit case.

If the input is certainly negative the digital output is a logic 0 and the DAC generates $-V_{ref}/2$. If the input is certainly positive the digital output is a logic 1 and the DAC generates $+V_{ref}/2$. In the uncertain region the output of the DAC is 0, midway between $-V_{ref}/2$ and $+V_{ref}/2$. Thus, the digital output corresponding to the grey region is midway between 1 and 0: half of 1. Using a second bit with lower weight we have 10, 01 and 00 for the three regions.

The correction of the ADC errors takes place in the digital block. This is why the method is called digital correction.

**Remember That**

The digital codes generated by a 1.5 bit ADC are only 10, 01 and 00. The code 11 is not used: the code 11 does not match any generated residual!
Fig. 3.28 indicates how the digital logic works. For 1-bit per stage the bits are simply delayed and placed side by side. A 1.5-bit per stage response uses adders to account for 01 outputs. The example of Fig. 3.28 c) assume that the third cell generates 01. The bit of the third cell is not fixed. The addition solves the value to 1 and corrects the result of the next fourth cell to 0.

Observe that the last residual generator does not use a three level ADC. The bit value in the uncertain regions is kept in an hold state. The first certain value of next stages solves this temporary hold. There is no cascaded stage for the last cell. This is why the LSB can not benefit of digital correction.

**Example 3.9**

Use behavioral simulation to study the ADC non-ideality of a a 1.5-bit per stage pipeline converter. Plot the residual response at the output of the first three stages. Assume errors in the thresholds of the first and second ADC only. Explain the achieved result.

**Solution:** The model file Ex3_9 and the m-file Ex3_9_launch enable the Simulink-Matlab simulation. The input ramp ranges -1 to +1. Each stage receives from the workspace five parameters: the two threshold of the ADC, the two levels of the DAC and the inter-stage gain. For the purposes of this example the DAC and the interstage gain are ideal. Thus, $V_{DAC,L}=-0.5$, $V_{DAC,H}=0.5$ and $Gain=2$.

The cascade of three stages provides the three residuals and the digital outputs. The ADC nominal thresholds are $V_{thL}=-0.25$ and $V_{thH}=0.25$. If the thresholds of the first ADC change to $V_{thL}=-0.16$ and $V_{thH}=0.18$ the residual, as shown in Fig. Ex. 3.9 a) exceeds the 0.5 level in the input range -0.25 to -0.16 and is below -0.5 from 0.18 to 0.25. The two thresholds identify the uncertainty region (0 at the ADC output).

The thresholds of the second ADC are $V_{thL}=-0.26$ and $V_{thH}=0.28$ the residual, as shown in Fig. Ex. 3.9 b) exceeds the 0.5 level in three regions of the input range and is below -0.5 in three other regions. The two arrows indicate the break points of the first stage. At these input values the residual of the first stage changes by 1. The ADC of the second stage swings from +1 to -1 and the effect of second stage DAC exactly compensates for the break transitions of the first stage residual.

The thresholds of the third ADC are correct: $V_{thL}=-0.25$ and $V_{thH}=0.25$. As a result the residual, as shown in Fig. Ex. 3.9 c) is within the ±0.5 limits in the central range of the input voltage. The break points of the second residual affect the ADC response. They cause ADC changes from 1 to -1. Since the shifted ADC transi-
Digital correction is also used in architectures with multi-bit per stage. The clipping of residual is avoided by reducing the interstage gain while maintaining unchanged the full scale range of the next stage. For typical values of mismatch it would be enough to slightly reduce the gain but the request of a binary
radix of the code points to a division by two of the gain.

Fig. 3.29 shows two possible plots of the residual of a stage with digital correction. Both figures refer to 4-bit and interstage gain equal to 8. The system of Fig. 3.29 a) divides the input range \((-V_{\text{ref}}, +V_{\text{ref}})\) into 16 equal segments. Assume that the output of the ADC is a four bits USB coding: \(b_3b_2b_1b_0\). With no ADC errors the residual is bounded in the \(+0.5\) - \(-0.5\) interval if \(V_{\text{res}}(-1) = -0.5\). The residual is \(-0.5\) at \(V_{\text{in}}(-7/8)\) and so forth. The corresponding DAC outputs are shown in Fig. 3.29 b). They are the midpoints of the ADC quantization intervals

\[
V_{DAC} = \frac{V_{\text{ref}}}{8}(8b_3 + 4b_2 + 2b_1 + b_0 - 7.5) \tag{3.32}
\]

where \(V_{\text{ref}}\) is assumed equal to 1. The DAC is required to generate 16 levels. They are shifted by half LSB with respect to 0.

Fig. 3.29 c) shows a second possible residual plot. The ending quantization intervals of the ADC are half LSB and the residual is zero at the boundaries of the dynamic range. The ADC uses 16 thresholds thus requiring 16 comparators instead of the 15 necessary for the solution of Fig. 3.29 a). The ADC identifies 17 intervals and the DAC must generate are 17 voltages. The USB coding requires an extra bit, \(b_4\), to code the last interval: 10000. The DAC outputs are

\[
V_{DAC} = \frac{V_{\text{ref}}}{8}(16b_4 + 8b_3 + 4b_2 + 2b_1 + b_0 - 8) \tag{3.33}
\]
Designing a 17 levels DAC and handling 5-bit can be problematic. If the first two and the last two quantization intervals are merged their amplitudes becomes 1.5 LSB of the 4-bit quantizer. The termination of the plot of the residual changes into the dashed lines. The ADC uses 14 comparators and the DAC generates 15 voltages. The change is valuable: apart from the first stage of the pipeline, the input of all the stages is well below the $\pm V_{\text{ref}}$ limits. It is not really necessary to extend the range of operation of the pipeline stage to the entire $\pm V_{\text{ref}}$ range. For the first stage an error in the $-3/16 V_{\text{ref}}$ and $3/16 V_{\text{ref}}$ thresholds can bring the residual outside the $\pm V_{\text{ref}}$ bounds. The limit possibly produces a clip of the input-output response but does not affect INL and DNL.

**Keep Note**

The cost of digital correction for multi-bit per stage is one bit less for every digitally corrected stage. The digital correction is not used in the last stage.

Observe that halving the interstage gain with an unchanged dynamic range reduces by one bit the effectiveness of the next stage resolution. Error free systems produce a residual response covering just over half the dynamic range. Thus, the MSB of the next stage does not provide information being always 0. Only errors on the ADC threshold give possible residual that exercise the MSB of the next stage.
stage. This is the way the error is detected and the limit compensated for. The
digital correction logic introduces proper delay to account for the timing of
the stages and adds the output of the stages overlapped by one bit to account
for the halved interstage gain. The result, as for the 1.5-bit case is not affected
by errors in the thresholds of the ADCs.

3.10 OTHER ARCHITECTURE

3.11 PROBLEMS

3.1

3.2

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